TRANSIENT OVERVOLTAGES ON SECONDARY WINDINGS OF MV/LV TRANSFORMERS DUE TO CAPACITOR ENERGIZATION - CORRELATION BETWEEN COMPUTED VALUES AND EXPERIMENTAL RESULTS

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ABSTRACT

Investigation have been made in such situation where low voltage capacitors, for power factor correction, are fitted very close from a MV/LV transformer. Due to the low impedance of the short busbars involved in the circuit between the transformer and the capacitor bank, high transients occur on the low voltage circuit with peak currents up to 35 times the normal capacitor current and peak voltages up to almost 2 p.u. Calculations using EMTP have been made previously from full power tests in laboratory. The results show very good correlation between computed and test results. Therefore computed model can be used in order to optimise the value of the pre-insertion resistance to minimise the transient over-voltages during the energization of shunt capacitor banks and so to reduce the dielectric constraints. This increases the life time of the installation and improves the power quality delivered to the users.

INTRODUCTION

Generally any switching operation, fault initiation, interruption, etc. in an electrical installation is followed by transient phenomenon in which overvoltages can occur. Since it is one of the most frequent system, switching operation capacitor switching overvoltages are an important type of switching overvoltage.

Energy conservation initiatives and power factor penalties increased the application of capacitor banks within both utilities and customer facilities for the purposes of power factor correction, energy losses reduction, voltage control and to release system capacity.

Capacitor banks energization gives rise of overvoltages close and also far away from the installation. These overvoltages can even be magnified on other location in the network.

The transient overvoltage magnitude is not severe for the transmission and distribution systems but can be a problem depending on the types of equipment within the end user system. Because of efficiency and flexibility improvement, customer loads such as computers, adjustable-speed drives, communications and medical equipment are being applied in increasing numbers. These types of load are the most common examples of equipment that may be very sensitive to capacitor energizing transient overvoltages ; nuisance tripping for adjustable-speed drives, computer problems (loose of data ...) and other customer equipment damage or failure. Numerous and frequent capacitor bank switching operations (for example for reactive power compensation of frequent load variations) can increase the (short or long term) impact on equipment.

The combination of increasing application of sensitive customer equipment and capacitor bank explains increased customer power quality problems due to capacitor switching transient and why the reduction of capacitor energizing transient overvoltages is of significant concern.

The most commonly used and effective mean to reduce low voltage capacitor energizing transient is pre-insertion resistance.

An optimal value of the pre-insertion resistance allows to minimise the transient overvoltages magnitude during the energization of shunt capacitor banks and so to reduce the dielectric constraints . This increases the life time of the installation and improves the power quality delivered to the users , who are more and more sensitive to electrical disturbances.

THE CAPACITOR ENERGIZING TRANSIENT

Capacitor switching is a normal event on utilities and customers systems.

When a capacitor with a residual (initial value) voltage equal to zero is energized there is an instantaneous short circuit (if no reactor is in series with the capacitor) or a voltage drop (a dip) at the bus voltage where the capacitor is located, because the voltage across a capacitor cannot change instantaneously. After this step wave change there is an oscillating transient voltage superimposed on the (50 Hz or 60 Hz) fundamental waveform because the energy oscillates between inductance and capacitance. Due to system losses and loads (resistive elements) the oscillatory component is damped and decays to zero generally in less than a half cycle (of the power frequency). The frequency(ies) of oscillations is(are) determined by the natural frequency(ies) of the circuit. The inrush current that flow into the capacitor is determined by the system impedances and is of the same frequency as the voltage surge. The peak voltage and current magnitudes depend on the closing instant in relation to the voltage of the supply system.

Maximum overvoltage :
The maximum of the first peak of the transient overvoltage is in the order of twice the peak magnitude of the system (nominal) voltage and occurs when a single capacitor (with residual voltage equal to zero) is energized at the peak of the supply system voltage wave and no capacitor in parallel already energized In case of capacitor residual voltage different from zero, higher overvoltages can be reached ; for example if the capacitor is fully charged to maximum voltage at the energization instant (due to the relative phase of current and voltage, when a switch interrupts the current at zero crossing, the voltage is maximum. The capacitor is isolated from the source and in case of no discharge device retains its charge) the overvoltage can approach a peak value of three times the peak magnitude of the system voltage.

Maximum peak inrush current $(\hat{I})$ and dominant frequency (f_S) of oscillation :
Single capacitor energization :
During single capacitor energization the peak magnitude and frequency of the inrush transient current are calculated as follows (Resistance are assumed negligible, capacitor residual voltages equal to zero and the three phases energized simultaneously):

$$\hat{I} \approx I_N \sqrt{\frac{2S}{Q}} = \frac{V_N \sqrt{2}}{Z} \quad (1)$$

$$f_S = \frac{1}{2\pi} \sqrt{\frac{1}{LC}} \quad (2)$$

Where :
I_N is the rated (r.m.s.) current of the capacitor (A) ;
S is the short circuit power (VA) where the capacitor is to be installed ;
Q is the rated output of the capacitor (VAR) ;
V_N is the supply phase to neutral (r.m.s.) voltage (V);
Z $\left(= \sqrt{L/C}\right)$ is the surge impedance of the circuit (Ω) ;
C is the equivalent star connected capacitance of the capacitor (F) ;
L is the inductance equivalent to the short circuit power S (H) $\left(L = 3V_N^2 / \omega S\right)$.

The oscillatory transient frequency f_S is between hundreds hertz and a few kilohertz.
Capacitor energization in parallel with energized capacitor(s) :
During capacitor energization with capacitor(s) already energized (back-to-back capacitor energization) the peak magnitude and dominant frequency of the switched on contactor inrush transient current are calculated as follows (Resistance are assumed negligible, the three phases energised simultaneously, the capacitances of the capacitor bank equal and the inductances in series with the capacitor equal):

$$\hat{I} \approx \frac{n}{n+1} V_N \sqrt{2} \sqrt{\frac{C}{L'}} \quad (3)$$

$$f_S = \frac{1}{2\pi} \sqrt{\frac{1}{L'C}} \quad (4)$$

Where :
n is the number of capacitor(s) already energized when the n+1 th capacitor is energized ;
L' is the inductance in series with each capacitors (H)

The oscillatory transient frequency f_S is the tens of kilohertz.

MODELLING

Investigation have been made in such situation where low voltage capacitors, for power factor correction, are fitted very close from a MV/LV transformer.
Calculations using the EMTP (Electromagnetic Transients Program) have been made previously from full power tests in laboratory.
Single line diagram of the three phase model used in the EMTP (in the frequency range of interest of the dominant transient oscillation) is given in Figure 1.

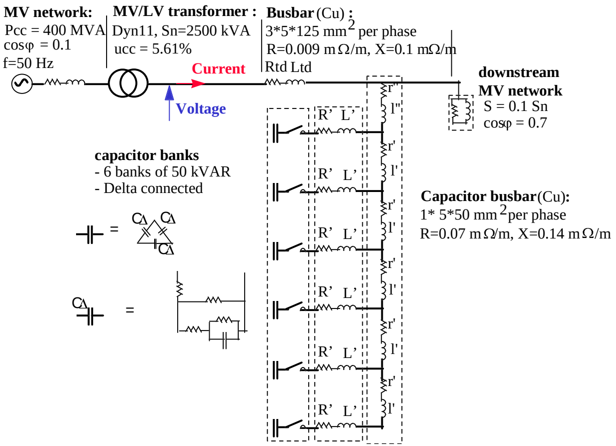


Figure 1 : EMTP model for capacitor bank energization

The MV supply network is modelled by a R,L series circuit calculated from the short circuit power and a three phase sinusoidal voltage source.
The MV/LV transformer (Dyn, 2500 kVA) is simulated by a linear (unsaturated) model that consist of three single phase units.
LV busbars are taken into account by their positive sequence impedances modelled by non coupled and lumped

R,L series circuits calculated from the geometry of the busbars.

The capacitor banks are modelled taking into account capacitor losses from dielectric, fuses, connections and discharge resistance.

Contactors are modelled by three time controlled switches closed simultaneously.

VALIDATION OF THE MODEL

Laboratory full power tests :

Laboratory full power tests which single line diagram is shown on Figure 2 have been performed at Les Renardières laboratory of EdF.

They include the variations due to :
- the making instant of the contactor,
- the use, or not, of an inrush limiting (pre-insertion) resistance on the contactor,
- and the number of capacitor banks energized.

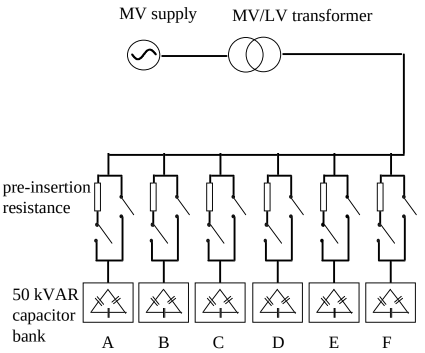
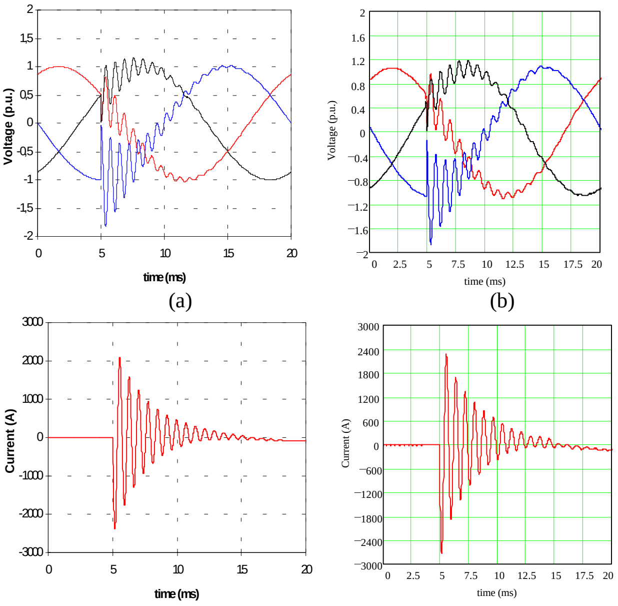


Figure 2 : Single line diagram of the measurement test

Validation of the EMTP model :

EMTP simulation results based on Figure 1 model show very good correlation between computed and test results. Examples of comparisons for the transformer LV windings voltages (phase to neutral voltages) and transformer secondary current are shown on Figure 3, Figure 4, Figure 5 and Figure 6.

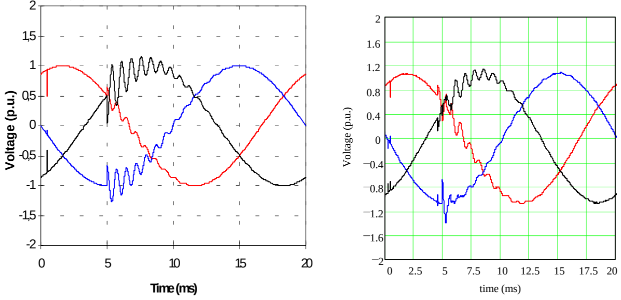
Due to the low impedance of the short busbars involved in the circuit between the transformer and the capacitor bank, high transients occur on the low voltage circuit with frequency around 1.2 kHz and peak currents up to 35 times the normal capacitor current, then higher than 2.4 kA (Figure 3c,d) and peak voltages between phase and neutral LV terminals of the MV/LV transformer, up to almost 2 p.u. (That is twice normal phase to neutral system peak voltage) (Figure 3a,b).



(a) (b)

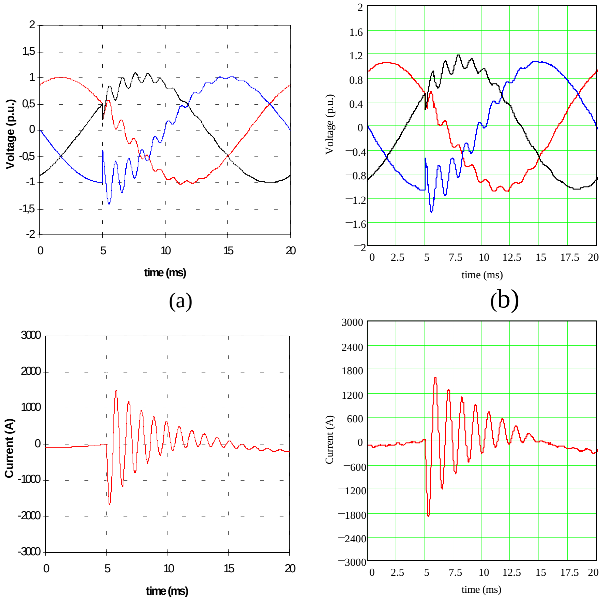
(c) (d)

Figure 3 : Energization of capacitor bank A with no pre-insertion resistance and no other capacitor banks energized : comparison between simulation (voltage (a) and current (c)) and measurement (voltage (b) and current (d).



(a) (b)

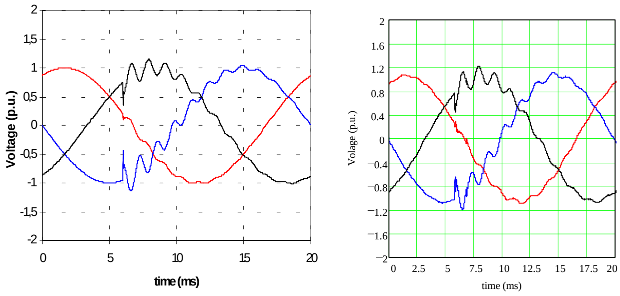
Figure 4 : Energization of capacitor bank A with pre-insertion resistance and no other capacitor banks energized : comparison between simulation (voltage (a) and measurement (voltage (b).



(a) (b)

(c) (d)

Figure 5 : Energization of capacitor bank A with no pre-insertion resistance and capacitor bank B energized : comparison between simulation (voltage (a) and current (c)) and measurement (voltage (b) and current (d).



(a) (b)

Figure 6 : Energization of a capacitor with no pre-insertion resistance and capacitor banks A and B energized : comparison between simulation (voltage (a)) and measurement (voltage (b))

EXAMPLE OF APPLICATION : OPTIMISATION OF THE PREINSERTION RESITANCE VALUE

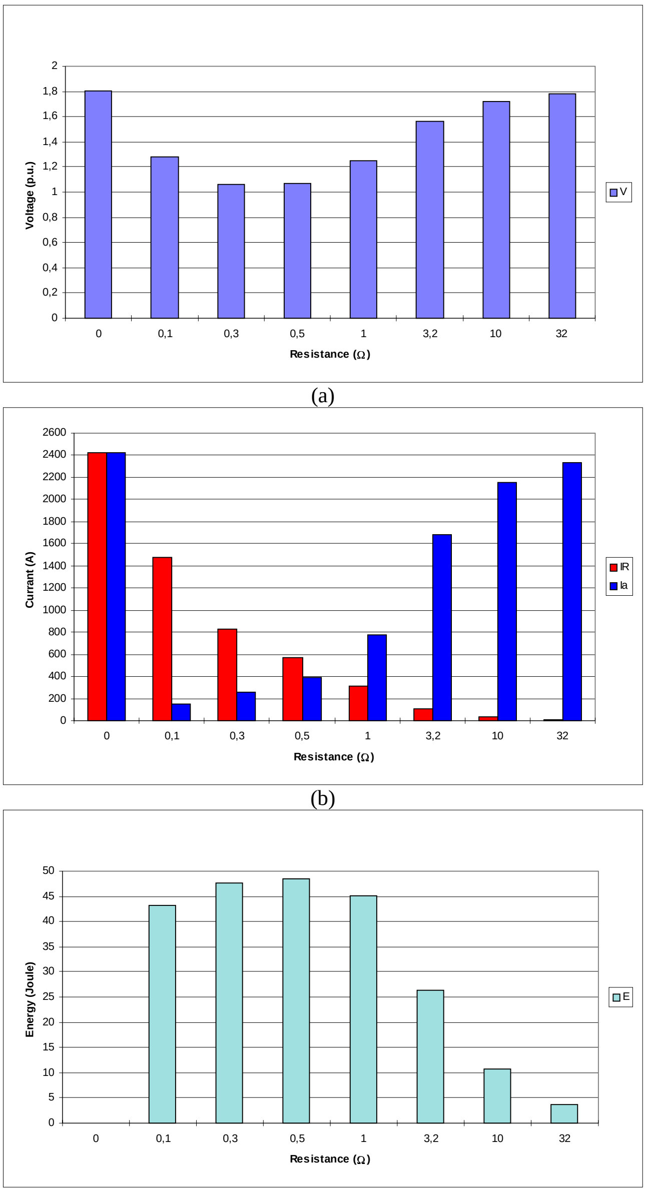
The most commonly used, effective and cost effective mean to reduce low voltage capacitor energizing transient overvoltages magnitude is pre-insertion resistance. Contactors designed for capacitor switching are equipped with a set of additional closing contacts and inrush limiting resistors. The resistances which decrease the initial transient magnitude are then bypassed producing a second transient (Figure 4). A well designed resistance provides a mean to reduce effectively the magnitude transient overvoltage well below 2 p.u.

An optimal value of the pre-insertion resistance minimising the transient overvoltages during the energization of shunt capacitor banks reduces the dielectric constraints. This increases the life time the reliability and the availability of the installation, lowers operating and maintenance cost requirements and improves the power quality delivered to the users, who are more and more sensitive to electrical disturbances.

The effectiveness of the pre-insertion control method is system parameters dependent. The computed model validated by comparison with measurements can be used in order to optimise the value of the limiting resistance and its thermal withstand for a given installation, considering the actual parameters of the MV and LV circuits.

For the example of the installation described on Figure 2, the influence of the pre-insertion resistance value on peak transient currents, transient overvoltage magnitude and energy dissipated by the pre-insertion resistance is studied for a single capacitor bank (with no other banks already energized) energized at maximum of the voltage on one phase. The optimum pre-insertion resistance value is around 0.6 Ω and minimise both the magnitude of the capacitor bank energization transient overvoltage from 1.8 p.u. (without pre-insertion resistance) to 1.1 p.u. (Figure 7a) and the inrush current from 2.4 kA (without pre-insertion resistance) to 400 A (Figure 7b).

The pre-insertion resistance thermal withstand depends on the pre-insertion time and the switching repetition rate.



(a)

(b)

(c)

Figure 7 : Example of application of the modelling : optimisation of the pre-insertion resistance value : (a) transient overvoltage magnitude versus pre-insertion resistance value, (b) peak current of the pre-insertion contact (IR) and the closing contact (Ia) versus pre-insertion resistance value, (c) Energy dissipated by the pre-insertion resistance versus pre-insertion resistance value.

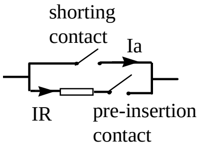


Figure 8 : current in shorting and pre-insertion contacts.

If the peak currents IR and Ia (Figure 7b and Figure 8) are not compatible with the current withstand of the pre-insertion contact and the closing contact, two contactors can be used. To avoid thermal failure of the pre-insertion resistance in case of the closure failure of the contactor that short-circuits the resistance, the pre-insertion resistance must be sized or protected properly.

CONCLUSION

Energy conservation initiatives and power factor penalties increased the application of capacitor banks within both utilities and customer facilities for the purposes of power factor correction, energy losses reduction, voltage control and to release system capacity.

The combination of increasing application of sensitive customer equipment (such as adjustable-speed drives) and capacitor banks explains increased customer power quality problems due to capacitor switching transient and why the reduction of capacitor energizing transient overvoltages is of significant concern. The most commonly used and effective mean to reduce low voltage capacitor energizing transient is pre-insertion resistance.

Investigation have been made in such situation where low voltage capacitors, for power factor correction, are fitted very close from a MV/LV transformer. Due to the low impedance of the short busbars involved in the circuit between the transformer and the capacitor bank, high transients occur on the low voltage circuit with peak currents up to 35 times the normal capacitor current, then higher than 2.4 kA, and peak voltages up to almost 2 p.u. (twice normal phase to neutral system voltage).

Numerous switching operations (for example for reactive power compensation of frequent load variations) can increase the (short or long term) impact on equipment.

Contactors designed for capacitor switching are equipped with a set of additional closing contacts and inrush limiting resistors.

The pre-insertion resistance thermal withstand depends on the pre-insertion time and the switching repetition rate.

One must be aware of a possible incompatibility between the peak transient inrush current reached for the pre-insertion resistance value that minimises the transient overvoltages magnitude and the current withstand of the shorting and pre-insertion contacts. In this case two contactors can be necessary and to avoid thermal failure of the pre-insertion resistance in case of the closure failure of the contactor that short-circuits the resistance, the pre-insertion resistance must be sized or protected properly.

Calculations using EMTP have been made previously from full power tests in laboratory. The results show very good correlation between computed and test results, including the variations due to the making instant of the contactor and to the use, or not, of an inrush limiting resistance on this contactor. Therefore, computed model can be used in order to optimise the value of the limiting resistance for a given installation, considering the actual parameters of the MV and LV circuits.

An optimal value of the reinsertion resistance allows to minimise the transient overvoltages during the energization of shunt capacitor banks and so to reduce the dielectric constraints . This increases the life time, the reliability and the availability of the installation, lowers operating and maintenance cost requirements and improves the power quality delivered to the users.