TECHNOLOGICAL CONVERSION TO "LEAD FREE" PRODUCTION: ASSESSMENT OF THE RELIABILITY FOR THE ELECTRONIC ENERGY METERS.

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INTRODUCTION

The UE has issued the directive 2002/96/CE (RoHS) concerning the restriction of the use of six hazardous substances in the production of electronic and electrical equipments. The substances are: Pb, Hg, Cr^{IV}, Cd, PBB, PBDE. Other Countries are adopting new legislations "RoHS like" that impose a global vision of the environmental load connected with the production of electronic devices. The incoming approach, for the electronic production, is "to the cradle to the grave". This new point of view means an epochal change of the technologies on which are based the production of electronic components and the process to solder them on the electronic boards. ENEL is a big consumer of electronic devices, more than 30 million electronic energy meters (in the following CE) have been designed, assembled and installed in the last four years. For this reason ENEL is strongly involved in this technological switching, and one of it's target is the assessment of the reliability of the electronic devices RoHS compliant (in the following Lead Free CE). Many fields in which the electronic is widely used theoretically got the exemption for the RoHS legislation. Any way the conversion process to the Lead Free seems to be not reversible and the Electronic Manufacturers prefer to manage only one type of production in their plants. This means that is possible to have Lead Free devices in application that theoretically and practically have the exception. For this reasons the results here presented may by interesting even for that Operator whose field up to now, is not involved in the Lead Free conversion (i.e. electro medical, heavy installation, devices working at high voltage).

RELIABILITY ASSESMENT METHOD

Due to the absence in literature of historical lead free data, ENEL decided to use, as base criteria, the comparison of reliability performances of the two technologies (SnPb vs. lead free) during the reliability assessment. The assessment path has been divided in five steps. First step: acquisition of the data sheets for the Lead Free components assembled on the CE electronic board. Second step: a survey, in technical literature, looking for information about the risks connected with the technological conversion. Third step: definition of the Process Criticality, Failure Mode, Failure Mechanism, related to the Lead Free CE. Every criticality has been evaluated with reference to papers coming from international technical literature. ENEL has assigned to each critically and Estimated Risk level (high - medium - low). The Estimated Risk level is based on the product of the following three factors: **i**. the probability that the Failure Mechanism will be activated ; **ii**. the severity of the potential damage; **iii**. the detectability of the damage before the CE will be installed. Fourth step: design and execution of a test plan that was able to activate the investigated Failure Mechanisms. Fifth step: comparison of the damages detected at the end of the test plan. Based on the evidences achieved during the assessment, ENEL finally identified the Expected Risk level for each Criticality/Failure Mechanism. The tests and the analysis has been carried out, under ENEL supervision, in the following laboratories: CESI [Centro Elettrotecnico Sperimentale Italiano], IMQ [Istituto Italiano Marchio Qualità], Top Rel.

INVESTIGATED FAILURE MECHANISMS

Here, in the following, is presented the list of investigated Failure Mechanisms. Even if they have been chosen expressly for the ENEL CE, they are representative for a wide number of general purpouse electronic devices.

Broken of the Inter-Metallic-Compound IMC: M1

Estimated Risk level	Criticality	Failure Mode	Failure Mechanism
High	Solder joint building	Loss of electrical connection	Broken of the IMC

The IMC is a zone in the inner of solder joint, stiff and fragile, composed by every metal presents at the moment of reflow. The reflowed metals could belongs to the solder paste, to the terminals of components and to the finishes of boards. The metallic and intermetallic bonds are obtained reflowing the solder paste. The final product of this critical manufacturing step is the creation of stable and reliable solder joint. The IMC available with lead free solder pastes has morphologic and mechanical properties very different from the properties of the IMC available with the traditionally SnPb solder paste. The Lead Free IMC is thicker and it shows the attitude to grow with temperature quicker than SnPb IMC. The aging process provokes on IMC mechanical stresses that produce the fatigue. When the IMC reaches the limit of supportable fatigue (the limit is function of thickness), appear creaks at interfaces IMC/terminal or IMC/PCB. This Failure Mechanism isn't reversible and it is amplified if the solder joint isn't made at the state of the art or if its dimensions aren't acceptable (reference standard: IPC A610-D). The Estimated Risk level is HIGH.

Component Delamination for IC and PCB: M2

Estimated Risk level	Criticality	Failure Mode	Failure Mechanism
High	Reflow step	Loss or modification of electrical functions	Broken of mechanical bonds between the basic parts (DIE/frame, barrel/dielectric)

The delamination is the loose of cohesion between basic parts which compose a functional element (Integrated circuit or board). The peak temperature and the time of permanence at liquid phase in the lead free soldering profile, are higher than in the old soldering profile. This fact provokes a higher thermomechanical stress, specifically on Integrate Components (IC) and on the boards (PCB).The cohesion of the layers that are the basic parts of IC and the cohesion between dielectric and metal parts in PCB are, during soldering in a very risky situation. It’s very difficult that this kind of damages are detected by test/inspection during the manufacturing process, for this reason the Estimated Risk level is HIGH.

Tin Whiskers Growth: M3

Estimated Risk level	Criticality	Failure Mode	Failure Mechanism
Medium	Component Plating	Electrical shock	Tin Whiskers growth

Tin Whiskers are electrically conductive structures that could grow on the surface of component’s terminals. The “RoHS” legislation has banned the Pb from the plating process of component’s terminal, not only from the soldering process. This fact amplifies the risk that the Tin Whiskers could grow-up. The growth’s mechanism isn’t reversible and the Tin Whiskers could reduce completely the isolation between electrical parts provoking electrical shocks on the devices. For the above reason the Estimated Risk level is MEDIUM.

Corrosion and loss of isolation : M4

Estimated Risk level	Criticality	Failure Mode	Failure Mechanism
Medium	Selection of chemicals	Interferences on measuring process	Corrosion of metallic parts

Acid residuals flux on the boards after soldering process could, in specific environmental condition, activate the corrosion process. In the lead free soldering process a bigger quantity of flux is used, and it’s more aggressive than the flux used in the traditionally soldering process. As a consequence the probability to have flux residual on board is much higher than in the past. The corrosion provokes the reduction of electrical isolation, and in the worst case, could interact with the main feature of the CE: the measuring process of energy. Estimated Risk level is MEDIUM.

TEST PLAN

The test plan implemented was based on 4 sequences of tests (each sequence is composed by test steps and analysis of the related results). The same number of SnPb and lead free CE were submitted to each sequence. In this way was possible to get a direct comparison between the two technologies.

SEQUENCE S1

This sequence was designed to study the Failure Mechanism M1 and M2 specifically for PCB. The sequence was composed by: **1.** visual inspection of solder joints; **2.** section of solder joint and inspection by microscope; **3.** thermal shocks; **4.** visual inspection of solder joints; **5.** section and inspection by microscope. (Reference Standard: IPC SM 785). The thermal shocks characteristics used to transfer thermomechanical stress to the solder joints were: temperature range → -40ºC+125ºC; Dwell Time → 7 minutes; gradient → 55°C/minute; nr. of thermal shocks → 500.

SEQUENCE S2

This sequence completes the previous one. The IMC’s thickness is the most important element for solder joints reliability, for this reason ENEL have decided to investigate also the IMC rate of growth during the normal life of devices. The devices under test have been putted at high temperature to accelerate the growing process. Micro sections of solder joints have been done before and after accelerated life test in order to valuate the IMC thickness. To measure the IMC thickness has been used the electronic microscope (SEM). The accelerating environmental conditions were: 125°C for 10 days.

SEQUENCE S3

This sequence was designed to study the Failure Mechanism M4 and M3. The sequence was composed by: **1.** accuracy test for the detection of the error in measuring process; **2.** Damp Heat test; **3.** repetition of accuracy test; **4.** visual inspection by microscope on component’s terminals looking for Tin Whisker. The environmental test conditions (Damp Heat test) were: temperature → 55ºC; Relative Humidity → 93%; test duration → 14 days.

SEQUENCE S4

This sequence was designed to valuate the Failure Mechanism M2 specifically for IC. The target was to valuate if the new soldering process induces latent damages on microprocessors. The method applied was the acoustic scansion of the component before and after the aging process. The sequence was composed by: **1.** acoustic scansion of IC; **2.**accelerated aging test; **3.** repetition of the acoustic scansion on IC. The environmental conditions for the aging were: temperature range → 0ºC +120ºC; Dwell Time → 7 minutes; average gradient → 4°C/minute; nr. of thermal cycles → 500.

EVIDENCES AND COMPARISONS

SEQUENCE S1

The thermal shocks activated the Failure Mechanism M1, both in lead free and SnPb solder joints. From the comparisons of the damages it's possible to say that the reliability of solder joints, for the two technologies, is comparable. The cracks in lead free and SnPb solder joints have the same dimension, even if the mechanism of propagation is quite different. This is due to the different metallurgical structure in the two kind of solder joints. Completely different is the assessment of the delamination in PCB (M2). These kind of damages are more frequently and wider in the PCB submitted to the lead free soldering process. The Figures 1 and 2 (SEM images) are taken from official CESI report (A6012076), requested by ENEL.

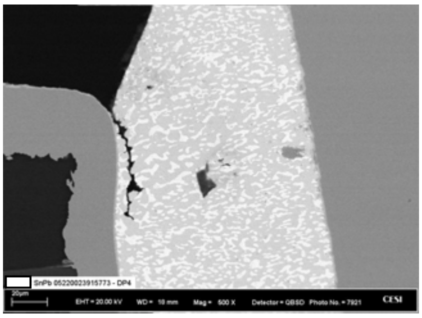

Figure 1: Cracked SnPb solder joint. It's visible a detail of Trough Hole solder joint. The crack goes in the solder joint and divides the grains of Sn from the grains on Pb. Another important item to remark is that the dimension of grain is bigger than before the aging test; this is a consequence of the application of the fatigue on the metallurgical structure of SnPb solder joint. It indicates that now the joint is more fragile. These two features are visible only in the SnPb solder joint.

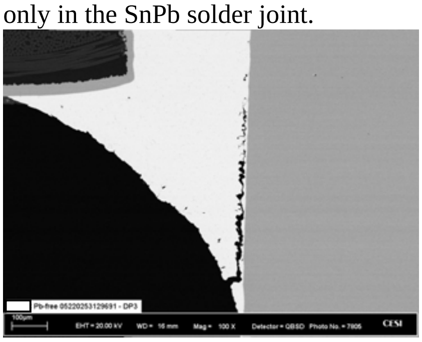

Figure 2: shows the SEM image of a joint, similar to the previous one, but realized with lead free process. The crack's dimension is comparable to the crack's dimensions in Figure 1, but here the propagation is in the IMC at interface solder paste/component terminal, not between the grains. The damages by delamination on PCB are more frequent in lead free process than in the traditional SnPb soldering process.

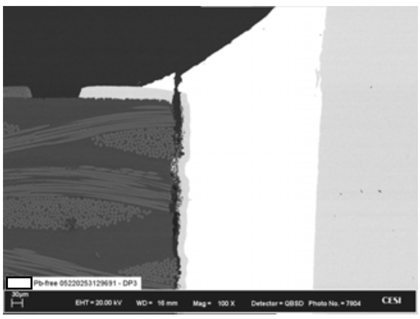

Figure 3: shows an example of delamination between a barrel (barrel is a metallized hole) and the dielectric material. This is due to the increased thermal stress in the lead free soldering process. This kind of damage wasn't found at all on SnPb solder joints.

SEQUENCE S2

This sequence starts and accelerates the growth of IMC. The IMC's thickness, before aging test, is double in lead free solder joints than in SnPb solder joints. Here the average values for IMC thickness were: 2 μm for SnPb solder joints; 4μm for Lead free solder joints. Also at the end of aging test the IMC thickness was double in lead free solder joints ,than in SnPb solder joints. The rate of growth is quite comparable for the two technologies: 30% for SnPb alloys; 40% for lead free alloys. The following figures are taken from official CESI report (A5054859). In these figures are underlined the IMC thickness, after a complete aging test.

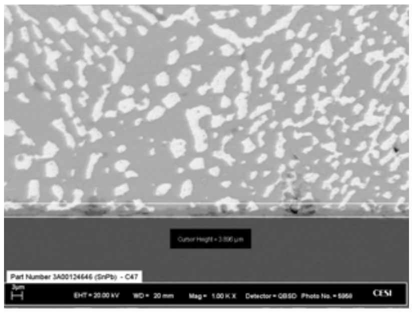

Figure 4: shows the IMC for a SnPb solder joints at interface solder paste /PCB. In the area delimited by white parallel lines is visible the diffusion of cooper in the solder paste occurred during the reflow step.

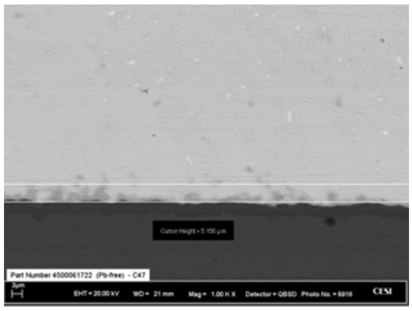

Figure 5: shows the IMC for a lead free solder joints, similar for packaging and dimensions with the component sectioned and reported in the previous figure. Even in this case the IMC at interface solder paste/PCB is delimited by the two white parallel lines

SEQUENCE S3

The Sequence S3 is related to the Failure Mechanism M3 (Tin Whisker) and M4 (active flux residuals). At the end of the "Damp Heat test" the boards have been inspected by electronic microscope and no metallic electrical conductive structures have been found on components terminals. The detection of error, in the measuring process, has been performed before and after the execution of the "Damp Heat test". The detected error shows that the measuring process is acceptable for both the kind of devices and, at limit, its more stable in the lead free one. In the Figure 5 is reported the graph of the detected error; in the y axis the variation of detected error before and after the Damp Heat test, in the x axis the ratio Voltage measured/maximum nominal Voltage. It's appreciable that the Delta error, for a lot of measure points, is minor in the lead free CE than in SnPb CE.
This is an unexpected situation. Must be underlined that the CE analyzed are preproduction devices and the

manufacturer has adopted all the expedients to reduce the quantity of flux applied on the board, and to deactivate it. In this effort the manufacturer has been supported by the choice to solder manually the Trough Hole components, rather in an automatic mode. It will be useful to repeat this comparison on mass production devices.

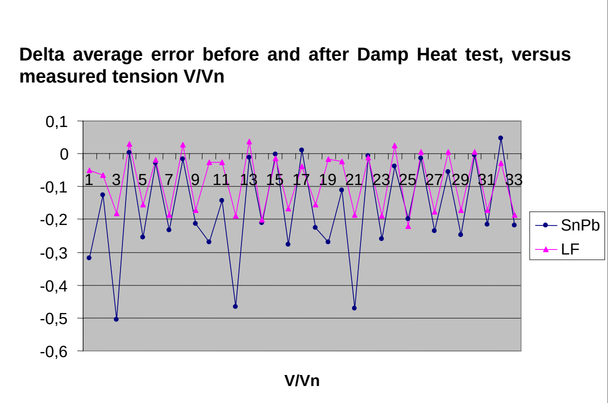

Figure 5

SEQUENCE S4

The Sequence S4 has showed an intrinsic fragility of the bond DIE/metallic frame in the lead free IC components. Before aging no delamination has been detected, while after aging a significant percentage of lead free IC presents a delamination at interface DIE/metallic frame. The acoustic image are taken from TopRel official report (ST- 0074TPR) requested by ENEL.

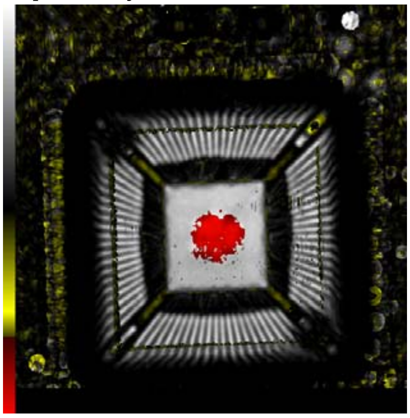

Figure 7 is the virtual image of one led free IC obtained by acoustic scansion in reflection mode. The red area is the source of a negative echo and it's generated by a delaminated zone. The time filtering process used during scansion permits to understand the depth at which is localized this delaminated zone.

A component like this one doesn't give the necessary guarantees of reliability for a long life time.

A similar damage, after only one reflow step and after aging test, underlines that the manufacturing process has no margins to tolerate the physiological fluctuation of soldering parameters.

FINAL CONSIDERATIONS

In the following table are reported the Expected Risk level and the end of the assessment related to the risk for every investigated Failure Mechanism:

Estimated Risk level	Failure Mechanism	Expected Risk level
High	M1	Medium
High	M2	High
Medium	M3	Low
Medium	M4	Low

M1 - The Expected Risk level isn't evaluated High because the aforementioned evidences show a similar behavior between the two different technologies, but the samples compared were not in the same state of art (lead free preproduction samples vs. SnPb end of production samples). For the above reason, ENEL decided to adopt a conservative approach, and doesn't put the Expected Risk level low. By the way in order to monitor this Risk the suggestion, after the validation of soldering profile, is to adopt a Control Manufacturing Plan capable to detect the quality of solder joint. On the other hand, the above evaluation isn't applicable if solder joint is contaminated by lead.

M2 - delamination: it has been demonstrated that the risk of delamination, both in PCB and in IC, is higher in the lead free technology than in the traditional SnPb process. The expected risk level is evaluated High because is very difficult to implement, in a mass production, useful inspections or tests capable to detect the damages provoked by this Failure Mechanism. The probability of an early fail on field, due to delamination, isn't negligible.

M3 – Tin Whisker: it has been proven that the risk, only for the assessed electronic board, isn't high.

M4 – Flux contamination: the results are encouraging; the risk is evaluated Low but the measure will be repeated with the mass production samples in order to double check the above consideration.

In conclusion the authors recommended reliability study in that fields where the expected performances, in terms of availability and precision, depend by electronic boards, even if at the moment those electronic devices benefit from the exemption to the RoHS directive.

REFERENCES

[1] H.J.Lau, C.P.Wong, N.C.Lee, S.W.R Lee, 2003, *Electronics Manufacturing with Lead Free, halogen-free & conductive – adhesive material*, McGraw-Hill Handbooks, City, United Stated of America.

[2] P. Juul, K. Zachariassen,T. Roslund, L. Ebdrup, B. Sloth, I. R. Nielsen, 1999, "Survey on lead free solder system", result of a Danish Environmental Protection Agency, project on the environmental and technical impacts of substituting lead containing solders by lead free solder system *COPENHAGEN 20-11-2002.*

[3] J.Oliver - Swedish Institute for metals Research "*Fatigue properties of Sn3.5Ag0.7Cu Solder Joints and effects of Pb-contamination*". *The Journal of SMT* Vol. 15, ISSUE 4, 2002