SURGE ARRESTER APPLICATION OF MV-CAPACITOR BANKS TO MITIGATE PROBLEMS OF SWITCHING RESTRIKES

Lutz GEBHARDT
ABB – Switzerland
lutz.gebhardt@ch.abb.com

Bernhard RICHTER
ABB – Switzerland
bernhard.richter@ch.abb.com

ABSTRACT

The paper presents the application of surge arresters as a switching overvoltage protection of capacitor bank circuit breakers. Based on an existing MV-Capacitor bank an EMTP-Simulation is performed to show the effectiveness of the surge arrester in reducing circuit breaker TRVs and in minimizing the probability of circuit breaker restrikes.
The energy requirements of the surge arresters and the overvoltage protection levels of the capacitors for different surge arrester arrangements are calculated.

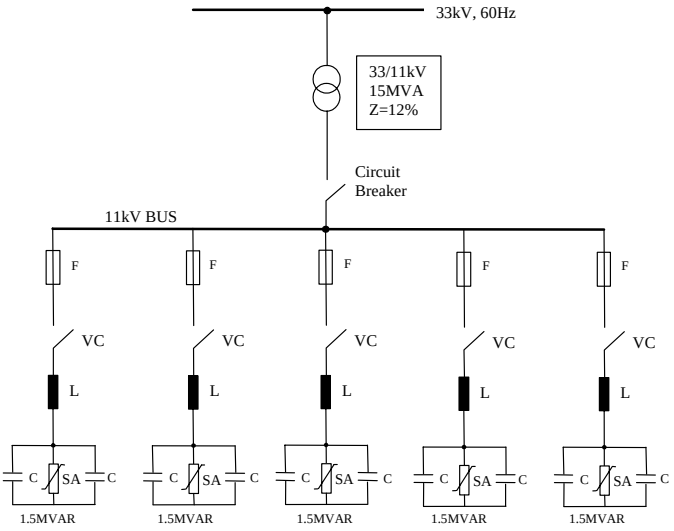
INTRODUCTION

Medium voltage capacitor banks are designed for industrial, utility and commercial power systems to improve power factor, increase system capacity, reduce harmonic distortion and improve voltage regulation.
Capacitor bank switching is one of the most demanding operations in MV networks, due to its associated transients. During the opening operation the transient recovery voltage (TRV) across the circuit breaker can rise to very high values and that can initiate breaker restrikes which in turn generate even higher overvoltages.
Consequently, any restrike implies additional stress for capacitor and circuit breaker, which reduces their lifetime or -in some extreme cases, if multiple restrikes occur- damages the capacitor and circuit breaker immediately.
A way to prevent these overvoltages for new switchgears is the installation of modern circuit breakers with a low probability of restrike. For users, having old existing switchgear not suitable for capacitor bank applications, the question is whether the inserting of surge arresters across the capacitor can minimize the probability of the circuit breaker restrikes.
Based on a real existing installation of a MV-Capacitor bank a study using the EMTP-RV Software was performed in order to evaluate the effectiveness of the surge arrester application in minimizing the probability of circuit breaker restrikes.

MODELLING

Based on an existing installation of a 5-stage, 11kV, 7.5MVAR capacitor bank (ungrounded double wye - connected), a 3-ph model of a MV-Capacitor bank including the network components (capacitors, reactor, circuit breaker, transformer) has been developed to perform an EMTP-Simulation for the opening operation of the capacitor bank. A single-line diagram of the capacitor bank is shown in Fig.1 with all the ratings marked therein. The modelling is based on the following conditions:

- The sequence of a three-phase break of capacitive load followed by restrikes in two phases at t=8.3ms (1/2 cycle) after current interruption was identified as the decisive case. The network with isolated neutral and a power frequency of 60Hz was selected as the most severe case
- The circuit breaker interrupts the high frequency current at the first current zero.



VC: Vacuum Contactor C: Capacitor 18.6uF SA: Surge arrester POLIM-H07
F: Fuse Link 180A L: Detuning Reactor 15mH

Fig.1: Single line diagram of the capacitor bank

- According Figure 2 three arrester arrangements are investigated: phase to neutral, phase to phase and phase to ground. The system neutral Rg was set to either zero or infinite
- As a surge arrester model a class 4 surge arrester type with a fixed protection level of $U_{RES}/U_C = 2.9$ (at I_N = 10kA) is used
- The magnitude of overvoltages is given in p.u. (per unit) as a multiple of the peak value of the line-to-ground voltage:

$$1\text{p.u.} = \frac{\sqrt{2}}{\sqrt{3}} \cdot 11\text{kV}_{rms} = 8.98\text{kV}$$

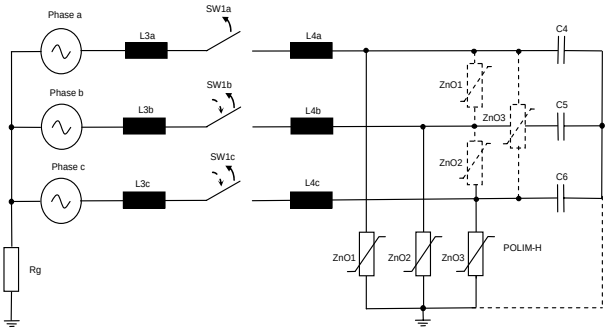


Fig.2: Equivalent circuit with the arrester arrangments: phase to ground, phase to neutral, phase to phase

DE-ENERGISATION OF CAPACITOR BANK

In order to evaluate the severity of overvoltages and to determine the effectivness of a surge arrester application, the step by step procedure was simulated for the following cases:

1. Three phase break of capacitive load
2. Three phase break of capacitive load associated with multiple breaker restrikes
3. Three phase break of capacitive load associated with multiple restrikes and using surge arresters
4. Comparison of breaker TRVs and capacitor voltages for the first pole-to-clear phase

1. Three phase break of capacitive load

Using the equivalent circuit according Fig.2 for a single-stage capacitor bank (S=1.5MVA) with no surge arrester connected on the network the voltage and current characteristics shown in Fig.3 are obtained. The first pole-to-clear is phase b and the circuit breaker SW1 interrupts the current in Phase b after t=11ms. From the moment the current is interrupted, the charge of the capacitor is trapped and the voltage remains constant at the value it had at zero current. The recovery voltage across the circuit breaker for the first pole to clear rises up to 2.5p.u.. This overvoltage is the most severe voltage stress for the circuit breaker for all investigated cases. As an assumption the circuit breaker is able to withstand the voltage stress of 2.5p.u. without a restrike.

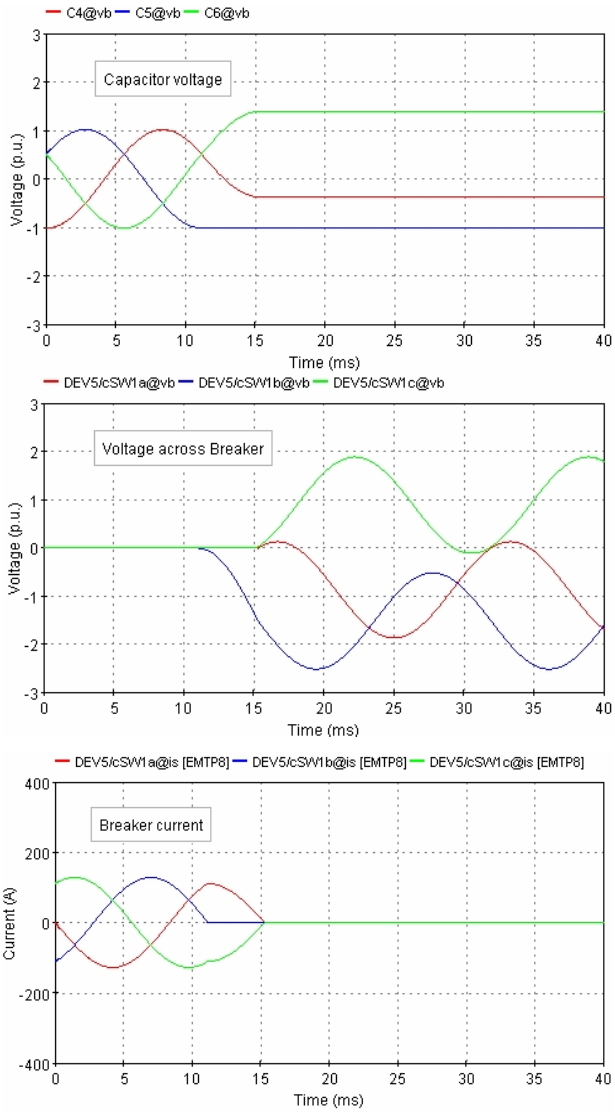


Fig.3: Three phase break of capacitive load

2. Three phase break of capacitive load associated with multiple breaker restrikes

The same sequence is simulated as in case 1 but as an assumption the circuit breaker is not able to withstand the voltage stress of 2.5p.u. and a two phase restrike occurs at the peak value of the recovery voltage at t=19.3ms in phase b and c (Fig.4). A transient current with an oscillation frequency determined by L3b/4b and C5 starts to flow and the voltage across the capacitor C5 swings up to 3p.u. The circuit breaker interrupts the current again at the first of its current zeros, with the result that the voltage across the capacitor C5 remains on the new constant value and voltage across the circuit breaker SW1 in Phase b and c rises up to 3.7p.u. after t=28ms. In case of further restrikes overvoltages will rise up to 6.1p.u. across the capacitors. This process of voltage and current escalation will damage the capacitor and breaker units

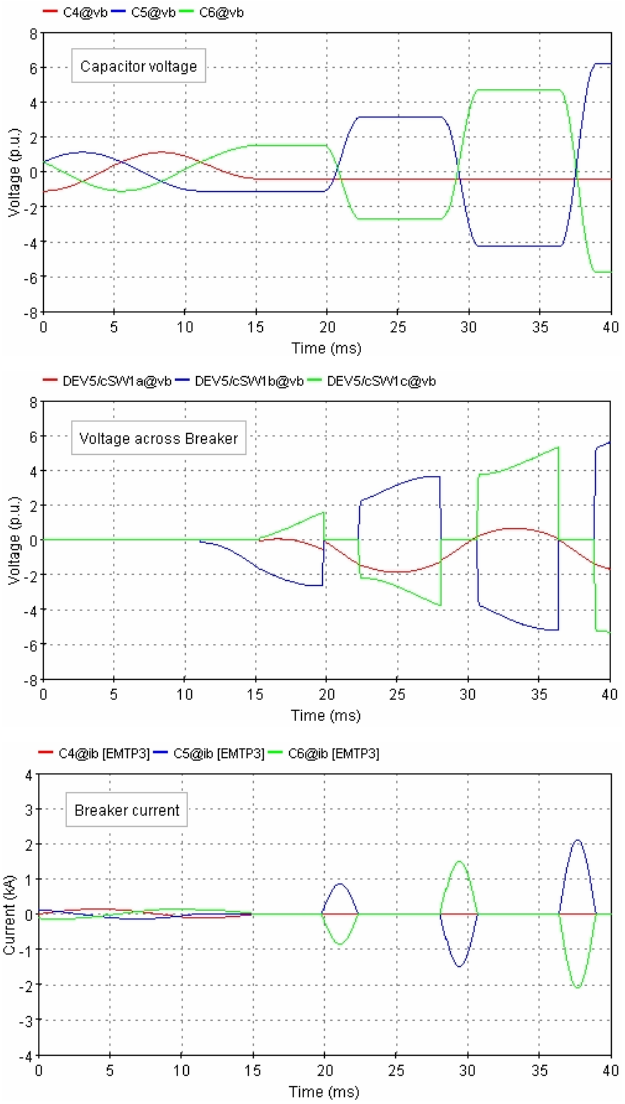


Fig.4: Three phase break of capacitive load associated with multiple breaker restrikes

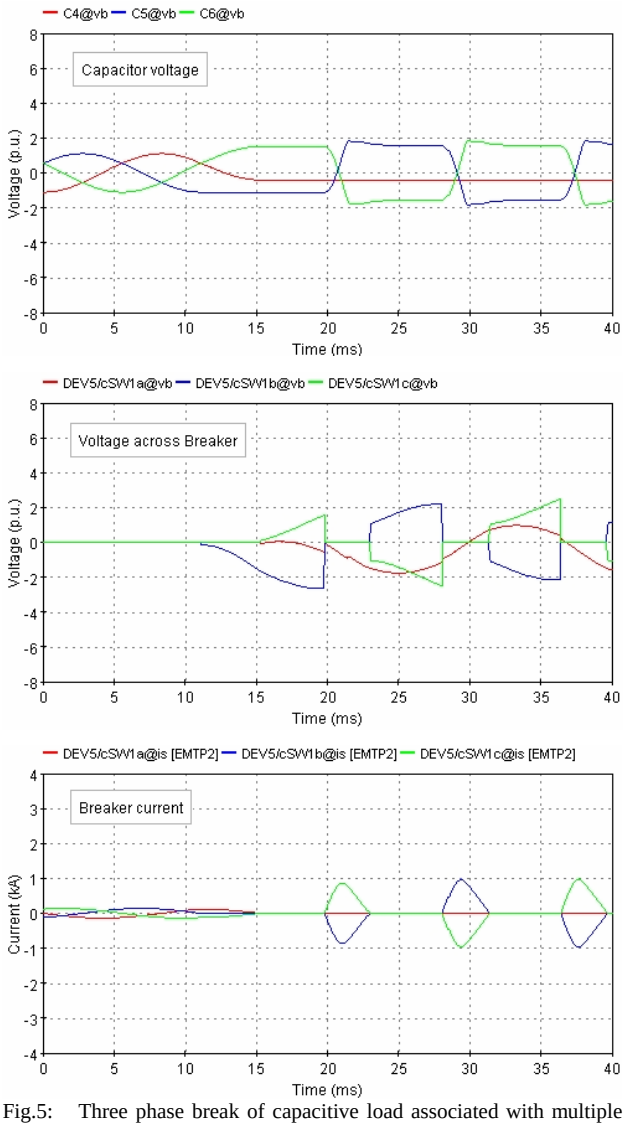


Fig.5: Three phase break of capacitive load associated with multiple breaker restrikes and using a surge arrester phase to neutral

3. Three phase break of capacitive load associated with multiple breaker restrikes and using surge arresters

The same sequence is simulated as in case 2 but using a surge arrester arrangement phase to neutral. The obtained voltage and current characteristics are shown in Fig.5. The surge arrester limits the overvoltage across the capacitors C5/6 at 1.9p.u.. In the case of multiple restrikes this overvoltage level remains constant. A voltage escalation across the capacitor and thus a capacitor failure is prevented.

The transient recovery circuit breaker voltage across the first pole-to-clear is limited at 2.1p.u. after the first restrike and that mitigates the risk of further breaker restrikes. The surge arrester not only protects the capacitor from dangerous overvoltages but decreases the probability of multiple restrikes of the breaker, too

4. Comparison of breaker TRVs and capacitor voltages for the first pole-to-clear phase

A detailed one-to-one comparison of the cases 2 and 3 for the first pole-to-clear (Phase b) characteristic shows the effectiveness of a surge arrester application (Fig.6). The effect of the TRV-limitation across the capacitor and the circuit breaker starts with the first restrike. There is no voltage limitation during the opening operation without a restrike. Therefore, the surge arrester can only reduce the overvoltages if a restrike occurs. There is no benefit for the circuit breaker to reduce the risk of a first restrike, but it mitigates the risk of multiple restrikes.

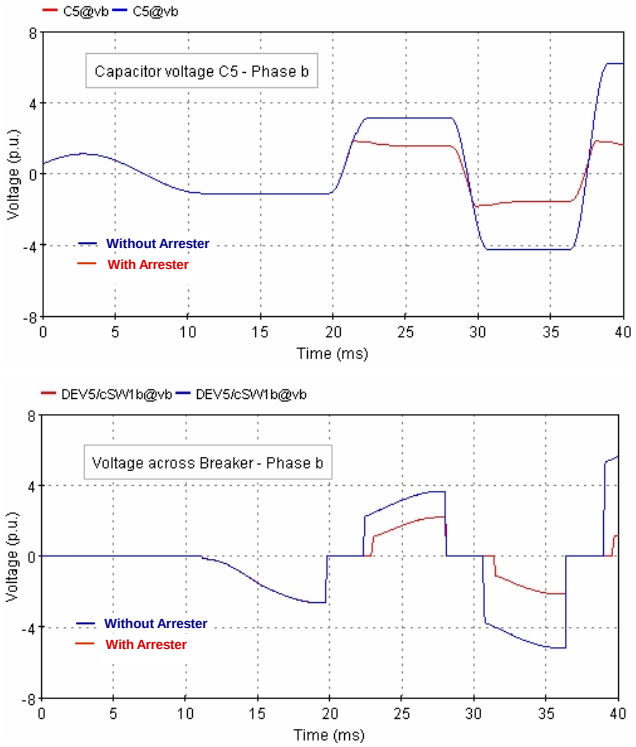


Fig.6: Comparison of breaker TRVs and capacitor voltages

ENERGY STRESS ON SURGE ARRESTER

The energy stresses on the surge arresters were calculated for different arrester arrangements (Fig.2) and different circuit parameters. The following results are obtained:

Energy stress as a function of the three phase capacitor bank size

A single-stage capacitor bank (Fig.1) is used to vary the three-phase bank size in order to evaluate the effect on the surge arrester energy stress.

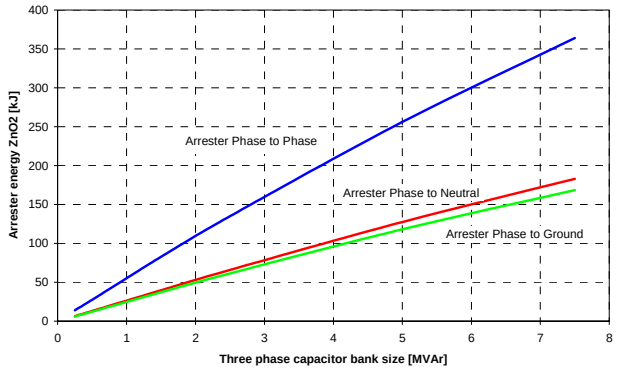


Fig.7: Energy stress as a function of capcitor bank size (based on 3 successive restrikes)

Depending on the arrester arrangement, a linear increase of the energy dissipated in the arrester is obtained.
The grounding conditions of the system neutral don`t effect the energy stress on the surge arrester. Only in case of a directly-grounded neutral (Rg ⇨ 0) and an arrester arrangement phase to ground a slightly higher energy of 7% has to taken into account.

PROTECTION CONSIDERATIONS

The voltages across the capacitor C5 of phase b for a single-stage capacitor bank is determined as a function of the three phase capacitor size. The resulting voltages depending on the arrester positioning are shown in Figure 8.

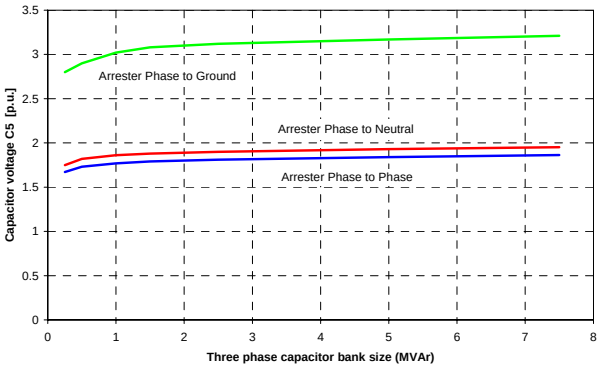


Fig.8: Resulting capacitor voltages as a function of capacitor size

The same capacitor voltage is obtained for systems with directly-grounded (R_g ⇨ 0) as well as ungrounded neutral (R_g ⇨ ∞).
The effect of the number of parallel capacitor stages and the number of repeated restrikes on the capacitor voltage is negligible.

CONCLUSIONS

Based on the computer simulation of the capacitor bank de-energisation the following application considerations and conclusions can be drawn:

- Using a surge arrester prevents a capacitor failure at a circuit breaker restrike by limiting the overvoltages across the capacitors
- Installation of a surge arrester mitigates the risk of multiple restrikes by limiting the TRVs of the circuit breaker

REFERENCES

[1] Stenström L and Mobedjina M, April 1995, "Guidelines for selection of surge arresters for shunt capacitor banks", *Electra*, Vol. 159

[2] ABB Publication, July 1999, "Dimensioning, testing and application of metal oxide surge arresters in medium voltage networks"

[3] Belanger J. and Menemenlis N., 1987, "Metal-oxide arresters as switching overvoltage protection of capacitor bank circuit breakers", *Colloquium paper CIGRE*, SC 33 (Tokyo) 03.05.