ACTIVE AND REACTIVE POWER FLOW CONTROL BASED ON D-SSSC FOR LOOPED AND MESHED DISTRIBUTION GRIDS

Erwan LE PELLETER
LEG / GIE-Idea – France
lepelleter@leg.ensieg.inpg.fr

Seddik BACHA
LEG / GIE-Idea – France
bacha@leg.ensieg.inpg.fr

Raphaël CAIRE
LEG / GIE-Idea – France
caire@leg.ensieg.inpg.fr

Joel GUIRAUD
LEG / GIE-Idea – France
guiraud@leg.ensieg.inpg.fr

ABSTRACT
The deregulation of the electrical market and the emergence of small energy production units connected to the distribution grid could induce a need on the one hand, to looped or to meshed some feeders and, on other hand, to control the active and or reactive power flows [1]. Series' connected Flexible AC Transmission Systems (FACTS) devices can control active or reactive power flows in the transmission system in order to share the power between lines, to reduce line’s losses or to avoid overloads for instance [2][5]. The aim of this work is to develop the control of an inverter connected in series to the distribution grid: a Distributed Static Synchronous Series Compensator (D-SSSC). A safe and reliable novel method which allows controlling the powers flows with no need to know line’s parameters is presented thanks to an automation approach.

INTRODUCTION
FACTS devices such as the Unified Power Flow Controller (UPFC), the Interline Power Flow Controller (IPFC) and the Static Series Synchronous Compensator (SSSC) can realize Power Flow Control (PFC) thanks to their series-connected converter. This is done through an adjustable phase and amplitude voltage inserted to the line in series.

The major goal of this system is then to control active and/or reactive power flow through the line, rather than the voltage injected. Thus, the desired power flow through the line should be ‘translated’ into the required injected voltage. Most of the theories on power exchanged with the line and/or reactive power flow through the line, rather than the voltage injected. The current has to be expressed (through his amplitude) as a function of the reactive voltage injected through the line ($v_{VSC}$). The approach uses in this paper lead to exploit Concordia and Park transformations [6]. Then the electrical values of the simple network in Figure 1 are expressed in the rotating frame synchronized with the current in Equation 1.

**Amplitude current control**
The first step which leads to the power flow control is the current control.

The control of the D-SSSC is synchronized with the line current thanks to a Phase Locked Loop (PLL), the voltage injected through the line will be $\pm \pi/2$ radians phase shifted. The current has to be expressed (through his amplitude) as a function of the reactive voltage injected through the line ($v_{VSC}$). The approach uses in this paper lead to exploit Concordia and Park transformations. The electrical values of the simple network in Figure 1 are expressed in the rotating frame synchronized with the current in Equation 1.

Figure 1 – Simple grid with D-SSSC
\[ \frac{di_d}{dt} = \left[ \frac{R_{\text{max}} + R_{\text{load}}}{L_{\text{max}} + L_{\text{load}}} \right] \omega i_d + \frac{1}{L + LcH} \left( v_{d\text{ feeder}} + v_{q\text{VSC}} \right) \]

**Equation 1**

Simplifications can be done as there is no \( i_d \) value due to the synchronization of the rotation frame. This leads to the expression of the amplitude of the current as a function of \( v_{q\text{VSC}} \) and \( v_{q\text{feeder}} \) in the Laplace domain. It can be seen that the transfer functions corresponding to \( v_{q\text{VSC}} \) the controllable variable and to the perturbation, \( v_{q\text{feeder}} \), are the same. Their particularities are to be constant and equal to the inverse of the reactive part of the grid impedance (Equation 2).

\[ \hat{i}(p) = i_d(p) = \frac{1}{(L + Lc\omega)} v_{q\text{VSC}}(p) + \frac{1}{(L + Lc\omega)} v_{q\text{feeder}}(p) \]

**Equation 2**

The equivalent bloc diagram of the grid can be shown as the following Figure 2.

![Figure 2 - Bloc diagram of the grid](image)

In the same way than the simplified grid, simplifications lead to the general expression, Equation 3:

\[ \hat{i} = i_d = \frac{1}{\sum_{n=1}^{m+1} L_n\omega} \left[ v_{q\text{VSC}} + v_{q\text{feeder}} - v_{q\text{VSC feeder}} \right] + \sum_{n=1}^{m+1} \left( \sum_{p=1}^{n-1} \left( \sum_{i=p}^{n} L_i\omega \right) \cdot i_{\text{load},p} - L_n\omega \cdot i_{\text{load},n} \right) \]

**Equation 3**

Each load and each voltage feeder appears as a perturbation but the transfer function keeps his properties (Equation 4).

\[ \hat{v}_{q}(p) = \hat{v}_{q}(p) = \frac{1}{\sum_{n=1}^{m+1} L_n\omega} \]

**Equation 4**

The optimal controller can then be chosen in order to have, in closed loop, a first order system (Equation 5).

\[ c_r(p) = \frac{K_r}{p} \]

**Equation 5**

First order systems present advantages: the output value will never exceed the reference value and the control is realized smoothly as there is no oscillations.

**Active or Reactive Power Flow Control**

The final goal of the system is to control active or reactive power. It is assumed that active and reactive power cannot be controlled at the same time as there is only one free controllable signal. So exploiting classic formulas of active and reactive power as a function of the voltage at the point of connection of the D-SSSC and the current through it, new expressions are obtained (Equation 6). These expressions are correct as it is assumed that voltage variations are low in comparison with current ones (especially in looped or meshed grid).

\[ \frac{p(p)}{v_{q}(p)} = \frac{3}{2} \frac{V_{\text{max}} \cdot \cos \phi}{\sum_{n=1}^{m+1} L_n\omega} \]

**Equation 6**

\[ \frac{q(p)}{v_{q}(p)} = \frac{3}{2} \frac{V_{\text{max}} \cdot \sin \phi}{\sum_{n=1}^{m+1} L_n\omega} \]

These expressions will be opposed to experimental results, (last part of the paper).

**DC BUS CONTROL**

Once, the rules of the power flow control have been set. The control of the DC bus device has to be done. Two methods are then proposed in the next section.

**Parallel control scheme**

The first control of the DC bus voltage is realized by direct action on the active part of the injected voltage. The voltage injected through the line is an image of the modulating \( \beta \) (or \( u \) when discretized) as the VSC can be seen as an amplification of \( \beta \) varying between -1 and 1 (the signal to amplify) by the gain \( Vd \) [6].

The first step is to express the current through the DC bus as a function of the active part of the modulator and the line current. See Equation 7.

\[ i_d = i \cdot \beta_d \]

**Equation 7**

\[ <i_d> << i \cdot u_d >\]

\[ <i_d> >= \frac{I_{\text{max}} \cdot u_{d,\text{max}}}{2} \]

This current flows through the DC bus and which is modelled by a resistor (\( R_c \)) in parallel with a capacitor (\( C \)). The evolution of the voltage can be obtained (Equation 8).

\[ \frac{v_{d}(p)}{u_{d,\text{max}}(p)} = T(p) = \frac{I_{\text{max}} \cdot R_c}{2} \frac{1}{1 + R \cdot C \cdot p} \]

**Equation 8**
It can be seen that the system is a first order expression. To control it, a PI controller can be chosen. With the compensation pole method, a first order system is obtained in closed loop (Equation 9) [6].

\[
OLTF(p) = C(p) \cdot T(p) = \frac{1 + \frac{\pi}{p} \cdot \frac{I_{\text{max}} \cdot R_c}{2}}{1 + \frac{\pi}{p} \cdot \frac{I_{\text{max}} \cdot R_c}{2}}
\]

\[
CLTF(p) = \frac{1}{1 + \frac{2\pi}{Kp} \cdot \frac{I_{\text{max}} \cdot R_c}{p}}
\]

**Equation 9**

The parameter \( Kp \) will be chosen in order to control the loading speed. However if this parameter is too high the apparent resistor of the system will reduce the current level \( I_{\text{max}} \) and make the load longer.

The global scheme for a single phase D-SSSC associating both power flow and DC bus control is presented in Figure 4. From the single phase scheme, the three phase scheme can be simply deduced with \( u_{\text{max}} \) and \( u_{\text{max}} \) directly sent to a SV-PWM [6] block synchronized with the line current.

**Figure 4 – Single phase control synoptic of the D-SSSC – Parallel control scheme**

**Inner loop control scheme**

The previous control scheme implies a DC bus voltage always set to his reference whatever the level of compensation of the impedance of the line. This induces non-optimal functioning as excessive losses are produce and non-minimal Total Harmonic Distortion reached. The DC bus voltage is not adapted to the require voltage needed to realize the compensation.

If the modulating \( \beta \) is always set to his maximum (amplitude close from 1) and the phase is shifted with the current by \( \pm \pi/2 \) radians (active power exchange null), an added phase shifting \( \gamma \) will create an active power exchange [5]. This will implies a non-null average current in the DC bus (Equation 10).

\[
< i_{\text{dc}} > = \frac{I_{\text{max}} \cdot u_{\text{max}} \cdot \sin \gamma}{2}
\]

**Equation 10**

The charge/discharge of the DC bus will be as high as the adding phase shifting will be important. A new system can be obtained as \( \gamma \) is the controllable variable to Vdc. A linearization of sin is considered; this one is justified thanks to low adding phase shifting evolution or the use of a linearized control (arcsin function). The transfer function is the one presented in Equation 11 which is very close to Equation 8.

\[
\frac{v_{\text{dc}}(p)}{\gamma(p)} = T(p) = \frac{0.95 \cdot I_{\text{max}} \cdot R_c}{2} \cdot \frac{1}{1 + R_c \cdot C \cdot p}
\]

**Equation 11**

The controller is the same than in the parallel control scheme. However as the control of the DC bus voltage is an imbricate control scheme the inner loop must be faster than the external looped which control the power flow through the line (Figure 5).

**Figure 5 - Single phase control synoptic of the D-SSSC – Inner loop control scheme**

The three phase voltage control obtained from the single phase voltage control is easy to obtain. \( u_{\text{dmax}} \) is set to \( \pm 1 \) there is an increase or decrease of the power flow and \( u_{\text{dmax}} \) is modulated continuously. These values are sent to the SV-PWM and the saturators adapt \( u_{\text{dmax}} \).

**EXPERIMENTAL VALIDATION**

**Test device presentation**

Both controls (parallel and inner loop) which have been presented in the previous sections were implemented in a low voltage grid (Figure 6). The SSSC is in series with a load.

**Figure 6 – General overview of the SSSC**

This one is decomposed into several parts:
- a feeder (400/230V);
- a physical SSSC is realized, thanks to three phases VSC associate to a filter (Table 1);
- a controller of the VSC is realized with dSPACE RTI1005. This device transforms Simulink schematics into C code exploitable by a DSP;
- a load, which is a three phase commutable variable load of resistor (6kW) and inductor (6kVar).

**Table 1 – Parameters of the physical SSSC**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Abreviation</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>LC filter inductor</td>
<td>LI</td>
<td>360 ( \mu )F</td>
</tr>
<tr>
<td>LC filter capacitor</td>
<td>C</td>
<td>100 ( \mu )F</td>
</tr>
<tr>
<td>Nominal apparent power</td>
<td>( V_{\text{dc}} )</td>
<td>10 kVA</td>
</tr>
<tr>
<td>Sample period</td>
<td>( T_s )</td>
<td>100 ( \mu )s</td>
</tr>
<tr>
<td>Commutated frequency</td>
<td>( f_r )</td>
<td>10 000 Hz</td>
</tr>
<tr>
<td>DC bus non voltage</td>
<td>( V_{\text{bus}} )</td>
<td>400 V</td>
</tr>
<tr>
<td>DC bus capacitor</td>
<td>( C_{\text{bus}} )</td>
<td>1100 ( \mu )F</td>
</tr>
</tbody>
</table>
**Parallel control scheme**

In Figure 8, the control of the DC bus to 400V can be observed (yellow: amplitude of the line current (A); blue: line current in phase 1 (A); green: voltage of the DC bus (V) and pink: voltage injected in series through the line (V)).

**Figure 8 – Parallel control scheme – Control of the DC bus to 400V**

The characteristic response of a first order system to a step reference is observed. The system behaves like a resistor as it absorbs energy. This is why there is a diminution of the line current.

In Figure 9 the control of the line amplitude current to 5A is presented. The characteristic response of a first order system can still be observed. The SSSC behave essentially as an inductor (see the phase shifting between the voltage injected and the line current).

**Figure 9 – Parallel control scheme – Control of the line current to 5A**

**Inner loop control scheme**

In Figure 10, the inner loop control is presented where the line is compensated in order to increase the line current. It goes from 9A, where the system behaves like an inductor, to 11A where it acts as a capacitor. The DC bus voltage level is adapted in accordance to the series voltage needed for the compensation.

**Figure 10 – Inner loop control scheme – Control of line current to 11A**

In Figure 11, the reactive power flow control is presented. It is decrease (blue) to 800Var following a first order step response as the active power flow naturally increases (yellow in Watt). The low evolution of the voltage in each part of the SSSC (pink and green in V) can be seen.

**Figure 11 – Inner loop control scheme – Reactive Power Flow control to 700Var**

**CONCLUSION**

In this paper, a novel method to realize power flow control thanks to a SSSC has been presented. This is a simple and generic method. Inner loop control scheme is preferred to parallel control as there is less harmonics and losses generation. The viability of the control has been experimentally checks and gives good results. SSSC for PFC seems to be interesting in looped / meshed network but the protecting scheme as to be revised because of the increase of short circuit current. The SSSC could be used to decrease the short circuit current in order to be still compliant with actual protection scheme.

**REFERENCES**


