INTELLIGENT UNIVERSAL TRANSFORMER DESIGN AND APPLICATIONS

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ABSTRACT

Legacy transformers are passive, bulky, becoming expensive, and take longer time to deliver. They cannot provide the power quality or control which today's loads demand for proper functioning and the electric system needs for its survivability. Solid-state transformers have been promising technologies in recent years. EPRI is pursuing development of an innovative solution – the IUTTM (Intelligent Universal Transformer), based on R&D100 Award winner SGTO devices, advanced thermalmanagement technology and packaging concepts to provide flexible, precise quality and reliable power at affordable costs. The IUTTM is a multi-function programmable power processing device ideal for Smart Grid and Sustainable Energy initiatives. This paper describes the design and application of this device.

INTRODUCTION

Conventional copper-and-iron based transformers have been challenged by solid state switching technologies in recent years [1-9]. A conventional transformer lacks energy storage capability, and thus the output load can be easily interrupted due to the disturbance at the input source. Similarly, when the output load current generates disturbances such as load transients, harmonics and reactive power, the conventional transformer also reflects them back to the input side. To overcome these problems, modern power electronics technology can be used to serve as the energy buffer between the source and load to avoid direct impact from either side.

EPRI is pursuing the development of an innovative new silicon-based device, the Super-Gate Turn-Off Thyristor (S-GTO) which promises to substantially increase the current rating and switching efficiency of power electronic controllers. An S-GTO can enable systems to be built using smaller devices with higher power densities and superior reliability. A major utility application of the S-GTO will be an Intelligent Universal TransformerTM (IUTTM), whose development is being driven by the rising cost of conventional transformers and the need to reduce the size and weight of their magnetic components.

IUT[™] is based on a number of technologies. The IUT[™] design is based on natural air convection cooling, eliminating expenses and problems associated with liquid cooling. S-GTO devices improve the power density by allowing higher frequency switching. They also improve efficiency by having lower conduction and switching losses.

S-GTO devices also have better thermal management which helps to make the IUTTM smaller and lighter. The S-GTO does not have wire bonding in its package, making it a significantly more reliable product. The IUTTM is also modular and scalable. By end of 2009, a 15kV class 100kVA 120/240V 1phase Pole-mounted IUTTM will be ready for field evaluation.

An S-GTO based Intelligent Universal Transformer (IUT^{TM}) is a promising enabling technology that can facilitate developments of future distribution systems as well as advanced distribution automation capabilities.

Major features are listed below as follows:

- Protection from on load disturbances
 - Instantaneous voltage regulation under load dynamics and transients
 - Maintain unity input power factor under reactive load condition
 - Maintain clean input under harmonic distorted or nonlinear load condition
 - Protection against unbalanced load condition
 - Protection against overload and output shortcircuit
- Protection from source disturbances
 - Voltage sag compensation
 - Outage compensation
 - Capacitor switching protection

In addition to the above power quality enhancement functions, with the flexibility of power electronics switching, the proposed IUT^{TM} can also include special outputs such as 48-V DC for telecom applications and 400-Hz for aerospace applications.

IUTTM CONCEPT

The work presented in this paper is a part of a multi-year effort to develop the high-voltage, multilevel converterbased intelligent universal transformer (IUTTM) based on an all-solid-state approach. The 2002 EPRI feasibility assessment [10] indicated that all these benefits could be realized only with an all-solid-state (power electronic) design that completely eliminates major inductive components from the overall design. In 2003, EPRI performed a comprehensive design and performance analysis of the IUT^{TMTM}, as described in *Development of a New Multilevel Converter-Based Intelligent Universal Transformer: Design Analysis* [11]. The essential performance parameters were derived and it was determined to proceed with the development of a laboratory bench model of the IUT^{TMTM}. In 2004-2005, a 20kVA 1-phase IUT^{TMTM} (20kVA, 2.4kV input and 120/240 output) laboratory bench model [12] was designed using power semi-conductor devices available in the market and tested to establish proof of concept for a suitable HV power electronic circuit topology for the IUT^{TMTM}. It was concluded to pursue the next phase of developing field prototypes and a commercialization plan from OEMs interested in IUTTM s.

The next phase of this multi-year project is to develop, test, and debug a field prototype and develop a specification for a first-generation product, taking into account the results of the field prototype research and development. By end of 2009, a 15kV class 100kVA 120/240V 1phase Polemounted IUTTM will be ready for field evaluation.

One may argue that the IUTTM will be much more expensive than the conventional one. However, the electronics can be designed with modularity and expandability. As compared to the conventional copperand-iron based transformer, the HV multilevel solid-state transformer will reduce transformer size and eliminate oil, aid in implementing "standardized transformer designs", enhance the power quality, and increase the functionality. When considering the enhanced functionality and flexibility, the added cost can be easily justified. In fact, the cost of power semiconductors and associated controls has exponentially decreased over the past decades. Especially with advanced wide band-gap materials such as SiC on the horizon for high-voltage devices, it is likely that the IUTTM will soon revolutionize the distribution transformer industry.

OVERVIEW OF THE STATE-OF-THE-ART SOLID-STATE TRANSFORMERS

To convert between two different voltage levels, it is necessary to have transformer isolation to fully utilize the silicon switches. Fig. 1 shows the use of a front-end boost converter for harmonic elimination, a full-bridge inverter for dc to high frequency ac conversion, a high frequency ac transformer for voltage level conversion, a diode bridge rectifier to convert high frequency ac to dc, and a fullbridge inverter to obtain low-frequency ac. Experimental waveforms are shown on top of each stage.

Consider Fig. 1 as a building block. The input of the building block is low-frequency high-voltage ac, and the output is a low-voltage ac with the same frequency. The power conversion is equivalent to a step-down transformer except that the power flow is uni-directional. This building block has been adopted in references [3–5] as a solid-state transformer module, and the entire system is to connect the input of several modules in series and the output of these modules in parallel. The circuit block diagram is shown in Fig. 2 where the top portion shows three modules using the

above-described circuit diagram, and the bottom portion shows how they are connected at the input and output. The main purpose of this configuration is to allow a highvoltage input that can be tied to distribution voltage level, and to have a low-voltage output that can be used for commercial and residential service.







Figure 2. Modularized solid-state transformer with series-connected input and parallel-connected output.

The major difficulty of implementing the circuit shown in Fig. 2 is to maintain the input voltage balance among different modules. With device mismatching and without any active control, the input voltages among different modules are unlikely to be maintained at the same level. One may argue that adding a set of voltage balancing zener diodes or clamping circuits will serve the purpose. However, the passive voltage balancing element or clamping circuit consumes a large amount of power and is not practical in high power applications.

Since the circuit topology of the basic building block is well known and is less of a concern, the main focus of the entire circuit design should be how to balance the input voltages among different modules. Unfortunately, this crucial problem has not been discussed in the literature. For distribution voltage level, the number of series connected modules is typically more than 10. The grounding and insulation between each module require special attention. The common-mode voltage for each module can also create nuisance tripping or faulty operation. Another problem with

this circuit is the component counts and their associated reliability issues.

With multiple-stage power conversion, each module already requires a tremendous amount of devices and components including semiconductor switches, gate drive circuitry, sensor and conditioning circuitry, and passive components. To accommodate the distribution voltage level with 7.2-kV line-to-neutral or 12.5-kV line-to-line using the abovementioned series connection for the input stage, it requires at least 15 modules for each phase and 45 modules for three phases assuming that 1200-V semiconductor devices are used for each input stage voltage with 480 V rms. Not only the balance of each input stage voltage is a problem, but also the component count can prevent the system from practically used.

EPRI IUTTM OVERVIEW

In order to overcome voltage sharing problem for series connected devices or converter stacks, several advanced multilevel converter circuit topologies have been discussed in [10, 11]. By incorporating advanced multilevel converters with the use of HV-Si devices (HV-IGBT were used for the bench model & HV-S-GTO is used for the field prototype) and SiC devices in the near future, it is possible to develop power converters for distribution system applications.

The proposed IUT circuit consists of a set of back-to-back interconnected multilevel converters to serve as both active-front-end (AFE) ac/dc and dc/dc converters, a high frequency transformer, and a dc/ac inverter. The input can be tied to high-voltage distribution system, and the output can be tied to low-voltage household applications.

For the field prototype, EPRI proposes the concept which combines a novel current mode resonant conversion circuit (rather than hard switching) with SGTO devices (rather than IGBTs or power MOSFETs) and SiC based Schottky diodes. Together, these provide low-loss, highly-reliable, low-stress circuits, resulting in smaller and lighter equipment.

The basic IUTTM circuit is shown in Figure 3.







The proposed design employs a circuit concept where multiple cascaded modulated H-bridges convert the 13.8 kV 60Hz AC into 3.5 kV DC at near unity power factor. Each 3.5 kV DC is then inverted into single phase 20 kHz AC by a series resonant converter using SGTO switches and Si-C Diodes. Voltage level transformation is achieved through a high frequency transformer. The resulting high frequency AC output of the transformer is rectified to 400V DC using a diode H-bridge. The 400V DC is then inverted to center tap 120/240V 1 phase 60 Hz AC using a hard switched inverter bridge. The outputs of the diode H-bridges are connected in parallel to achieve the desired power level. Each resonant converter output is a current source to the load so these are also connected in parallel. The high frequency transformer also provides galvanic isolation. This configuration of resonant converter that uses the leakage inductance of the high frequency isolating transformer as the resonant circuit L is inherently suitable for high voltage isolation applications since the required leakage inductance makes it possible to use a substantial isolating layer between input and output windings. The modularity of the design is evidenced by the use of the 25kVA building blocks.

The IUTTM design also employs external natural air-cooling, eliminating the expenses and problems associated with liquid cooling. SGTO can further improve power density and cost by allowing the switching frequency to run up to 50 kHz (compared to IGBT limitation of 20 kHz max). SGTOs also have lower conduction losses (50% of that of IGBTs) and lower switching losses (50% of that of IGBTs). In addition to lower losses, SGTO devices have better thermal management (lower thermal resistance) compared to IGBT or other power switching devices, ultimately making the equipment smaller, lighter and less cost. Since IGBTs do not have wire bonding in their package, SGTO modules have 100 times better reliability than IGBT modules. SPCO's concept further optimizes the design by using Si-C anti-parallel diodes with almost no switching losses. The design concept is modular and scalable, providing quality, reliability and economy of scale.

EPRI IUTTM Design

The packaging of the IUTTM is modular for ease of manufacturing and service. Figure 4 shows the proposed pole-mounted enclosure. The component layout inside the enclosure is optimized for electrical and thermal performance, and for ease of manufacturing and access. Access doors are provided on one side. The control system will be designed for continuous diagnosis of the IUTTM. A local operator interface will be provided. High-voltage bushings are mounted on the top for ease of connection and the output termination is provided on the side.



Figure 4: 100 KVA IUTTM Outline (Pole Mount Layout) - 35"H 35" W 20"D, 1050 lbs

EPRI IUTTM Design Features

The IUTTM follows a modular design (see Figures 5-7) incorporates the following features for performance, ease of operation, installation, troubleshooting, and life cycle cost.

- Use of low loss and reliable SGTO devices as shown in figure 5
- Higher frequency switching for compact foot-print
- Resonant switching for less stress on devices
- Modular design as shown in figure 6 & 7
- No mineral oil
- Sealed Compartment for Electronics components
- Robust construction for outdoor applications



Figure 5: R&D100 Award Winner SGTO Device

The power electronics components are arranged in four separate stacks, each rated at 25kVA. Each stack (see Figure 6) consists of an active front end (a level of the cascade converter) and a resonant converter. Each stack has a high frequency transformer. One stack includes the output inverter. The control boards and bus bar then overlay the power electronics. Each 25kVA stack contains all necessary electronic components such as capacitors, inductors and resistors that are required for operation of the system.





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Figure 7 100KVA System

100KVAIUTTMPERFORMANCESPECIFICATIONS

Parameters [13], [14]

| • | Input Voltage, kV rms | 15kV |
|---|---|---------------|
| • | Input transient Voltage, for 1 cycle | 130% |
| • | Power Frequency, Hz | 60 |
| • | Line power factor control | > 0.98 |
| • | Input current Harmonic control | < 5% THD |
| • | Output Voltage, V rms | 120 - 0 - 120 |
| • | Output voltage regulation | +/- 2% |
| • | Output Voltage Harmonic Distortion | < 5% THD |
| • | Output current, A rms | 417 |
| • | Fault current, A rms for 1 cycle | |
| | 2000 | |
| • | Dielectric Withstand | |
| | Power Frequency 1 min, kV rms | 34 |
| | Impulse, Full-wave, kV peak | 95 |
| | – Impulse, Chopped-wave, kV peak | 110 |
| • | Max. Ambient Temp, Degree C | 40* |
| • | Power Efficiency | 94% |

*Derating for higher ambient temperature

IUT PERFORMANCE VERIFICATION

Initial verification of the performance of the IUTTM was achieved through a series of simulations performed at various load and input conditions.

The following performances were verified:

- Instantaneous voltage regulation under load dynamics and transients
- Maintain unity input power factor under reactive load condition
- Maintain clean input under harmonic distorted or nonlinear load condition
- Protection against unbalanced load condition

- Voltage sag compensation
- Capacitor switching protection
- Protection against overload and output short-circuit

Figures 8 through 15 show responses to load and source disturbances.



Figure 8 Input Current vs Input Voltage



Figure 9 Output waveforms of the $\mathbf{IUT}^{\mathrm{TM}}$



Figure 10 Unbalanced Output Waveforms vs Input Voltage/Current



Figure 11 Fully Switched Unbalanced Load vs Input Voltage/Current



Figure 12 Voltage Sag and Its Effect on the Input Current/Voltage



Figure 13 Non-linear Loads vs Input Voltage/Current



Figure 14 Capacitor Switching Transient vs the Output Voltages/Currents



Figure 15 Load Step Transient vs Input Current

SUMMARY

The rapidly rising costs of the conventional transformers, the need for reducing the size and weight of the magnetic components, the need for distribution automation and monitoring to improve reliability, the requirements for new services, and the need to meet customers' power quality and reliability requirements have driven possible alternative solutions to the conventional transformer. This paper has proposed the concept of a solid-state transformer which has the potential and feasibility to provide a solution to above mentioned needs of the utility power delivery system.

The development of the IUTTM will provide an opportunity to offer DC service, high-frequency AC service, and the ability to convert single-phase service to three-phase for supplying customer loads in areas not served by three-phase circuitry. The ability to provide a wide range of services and improved operational benefits has put solid-state transformer technology - an Intelligent Universal Transformer (IUTTM) - in the forefront of this endeavor.

The IUTTM represents a promising new technology that can impact a wide range of applications. These applications are summarized in Figure 16.



Figure 16 Applications of IUT in a Smart Grid Interface

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MISCELLANEOUS

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Arindam Maitra (M'1995) received his BEE and MS, and PhD degrees from Nagpur University and Mississippi State University in 1995, 1997 and 2002, respectively. Arindam Maitra is a senior project manager in the Energy Utilization program area of the Power Delivery and Utilization (PDU) sector at the Electric Power Research Institute. He is currently responsible for leading and managing activities related to power system infrastructure requirements for Plug-in Hybrids. He is also responsible for conducting and managing numerous research activities

associated with power systems and power electronics. Prior to joining the Electric Transportation Group in EPRI, Arindam Maitra worked as a Senior Project Manager in the System Analysis and System Studies Group at EPRI (previously EPRI Solutions and EPRI PEAC). He was responsible for conducting and managing a wide range of research activities and power system studies in the transmission, distribution, PQ, and IntelliGrid research areas. He has managed a variety of projects related to reliability improvement, power electronic development efforts, indices for describing power quality and reliability performance, and load model development. He was also the project leader for a variety of load modeling research projects, including the projects involving air conditioner testing, at EPRI Solutions. He has supervised the development of advanced load models based on air conditioner test results and based on actual field measurements of aggregated load response to disturbances.

Ashok Sundaram is a Senior Project Manager in the Power Delivery and Utilization Sector at EPRI. He is currently managing development of the first distribution-class 15-kV Solid State Current Limiter (SSCL) using Super Gate Turn-Off Thyristor (SGTO) technology. He is also the project lead in a U.S. Department of Energy sponsored effort to build a 69-kV transmission class SSCL using SGTO's. Since joining EPRI in 1993, Mr. Sundaram has managed a broad range of projects to develop sophisticated, highly-advanced power electronics and system monitoring devices in both transmission and distribution applications. These projects include an innovative Distribution Fault Anticipator (DFA), the world's first platformmounted Dynamic Voltage Restorer (PMDVR), the world's first Advanced Static Var Compensator, and the world's first Distribution Static Compensator (DSTATCOM). Extensively published on these groundbreaking efforts, Mr. Sundaram was an EPRI 2007 Chauncey Award winner, and was an R&D 2007 award recipient for the SuperGate Turn-Off Thyristor. Before joining EPRI, Mr. Sundaram worked as a Power Plant Engineer at the Ennore Thermal Power Plant in India; as an Applications Engineer at Behlman Electronics in Carpenteria, California; and as a Senior Applications Engineer at Elgar Corporation in San Diego, California. Mr. Sundaram holds a BS degree in electrical engineering from the University of Madras in India and an MS degree in electrical engineering from Southern Illinois University at Carbondale.

Mahesh Gandhi is the General Manager of Silicon Power. He received his BS in Electrical Engineering from Gujarat University, India in 1982 and holds a PE license. He is a member of the IEEE. Prior to joining Silicon Power he was Engineering manager at L-3 / SPD, PA where he developed a Power Node Control Center (PNCC) Power Node Delivery Center (PNDC) for use in Naval Shipboard use, Wayside Indoor metal-clad switchgear 150kV BIL and 250kV BIL, Submersible Network Protector for use in ConEd and a Solid-state circuit interrupter. Prior to joining L-3, he worked for Inductotherm, NJ as a Lead Product Engineer and for Hind Rectifier, India as an Electrical Engineer.

Simon Bird is a Principal Engineer with Silicon Power. He received his BS and PhD in Physics from Manchester University, UK in 1995 and 1998 respectively. He manages Silicon Power's Systems group and is involved in the SSCL and IUT projects. Prior to joining Silicon Power, he was Controls / Electrical Engineering Manager at Inductotherm, NJ, a capital equipment manufacturer for the foundry industry where he worked on their inverter based furnace power supplies and automatic pouring systems.

Shoubhik Doss is a Project Engineer with Silicon Power, working as technical lead on the IUT project. He received his BEng in Electrical Engineering from University of Mumbai in 2005 and his MS from NCSU in 2008. Prior to joining Silicon Power, he worked as a Research Assistant at the Semiconductor Power Electronics Center in NCSU. His main focus was the electro-mechanical and thermal design of power converters with optimized parasitics.