ELECTRICAL NETWORK TESTING AND SIMULATION: AN EFFECTIVE METHOD OF TESTING THE FAULT RIDE THROUGH CAPABILITIES OF PROTO-TYPE EMBEDDED GENERATION

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ABSTRACT

The UK electrical networks are facing changes with regards to the uptake of a greater number of integrated distributed generators, (DG). DG can result in bi-directional power flows, change in grid losses, change in fault levels and require variation of grid protection. With an increasing number of DG units many network operators have defined mandatory 'fault ride through' requirements, resulting in generators maintaining connection during system disturbances. This means that the generation must withstand a 'low voltage ride through profile'. This paper presents a simple and effective method in the laboratory of varying the fault / voltage dip profile to determine the generator under test conforms to the appropriate ride through requirement profile

INTRODUCTION

A small electrical network, designed to test small scale proto-type generators has been set up in the Narec laboratory. The generator under test was subjected to various fault conditions, i.e. 3-phase, 2-phase, 1-phase and phase to phase faults. A simple test method was adopted to adjust fault level, voltage dip and fault duration to test the performance at any or every point along the ride through profile, giving the option to clear the fault at any time as well as controlling the voltage recovery. Once set up, a single test can verify that the generator under test conforms to the appropriate low voltage ride through profile requirement.

VOLTAGE-DURATION PROFILE LOW VOLTAGE RIDE THROUGH (LVRT) REQUIREMENT

The voltage duration LVRT requirement varies from country to country, mainly aimed at grid connected power stations, particularly wind farms. The UK National Grid Code specifies LVRT requirements for 275kV and 400kV transmission systems. The NGT grid code defines that (a) for short circuit (S.C.) faults at supergrid voltage each generator unit should remain transiently stable and connected to the system without tripping for a close up solid 3-phase fault or any unbalanced S.C. fault, for a total fault clearance time of up to 140ms and (b) for balanced supergrid voltage dips having durations greater than 140ms

and up to 3 minutes each generator unit should also remain transiently stable and connected to the system without tripping. The NGT LVRT voltage duration profile requirement is shown in Fig 1a. Note that Fig. 1a displays a boundary to which a generator with fault ride through capabilities must remain connected within the operating region above this characteristic. It must be disconnected from the network if it drops below this curve.
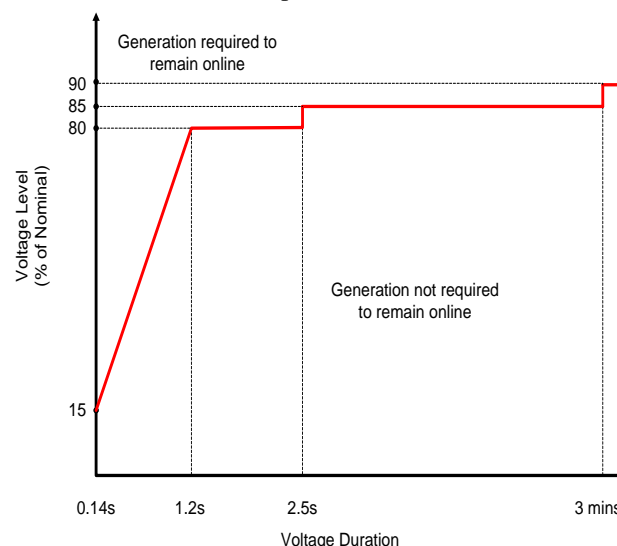

Fig. 1a

CENELEC is a European working group aiming to harmonise the requirements for the connection of embedded generators rated above 16A to MV and LV distribution networks. Fig. 1b shows a CENELEC fault ride through profile. For the tests outlined in this paper it is this fault ride through profile that has been replicated in the laboratory to ensure that the test generator remains connected during the fault period.
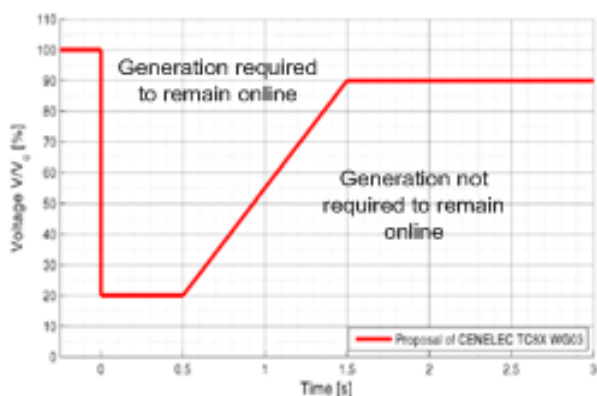
Fig 1b

FAULT SIMULATION IN THE LABORATORY

Narec is an independent centre for the development, testing and commercialisation of next generation technologies relating to electrical networks, wind, wave and tidal generation as well as the impact these technologies have on the interconnected power system to which they connect.

Recent laboratory tests have been carried out on small scale embedded generators to investigate their performance under adverse network conditions such as faults and voltage depressions. A test rig was setup in the laboratory to replicate a small electrical network comprising of a grid supply, some embedded generation and a load. Fig. 2 shows the network layout.
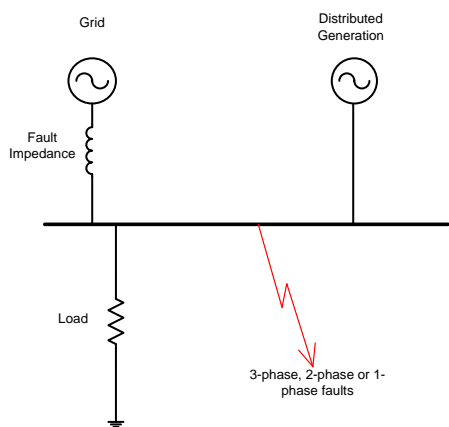

Fig. 2

A laboratory network schematic diagram is shown in Fig. 3 using the following components;
- Passive components, i.e. an adjustable resistive load bank and adjustable inductances to control the fault level
- Simple timers to initiate the fault, vary the fault duration and control the fault impedance
- Electrical machines to represent the grid and vary the fault impedance

The star points on the grid machine, test generator, the induction machine in the fault path and 3-phase load are all connected together to form a common neutral, as shown in Fig. 3 such that the network operates independently from the building supplies.
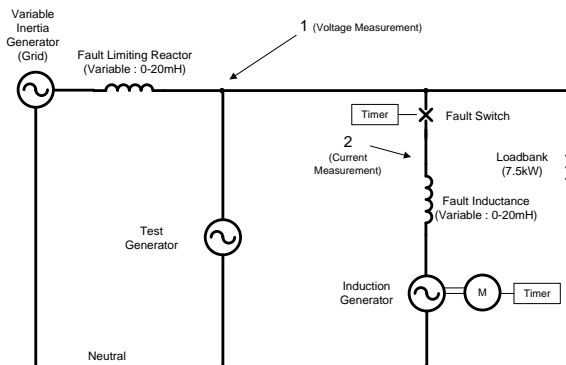

Fig. 3

The voltage profile can be altered by varying the fault impedance using additional induction machine in the fault path and running the machine up to speed when the fault is initiated. This is done via an industrial drive unit controlling a drive motor. Fig. 4 shows the generator impedance-speed characteristic.
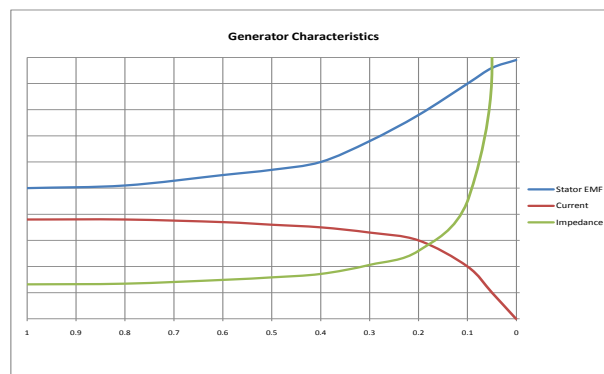

Fig. 4

COMPUTER SIMULATION FOR A 3-PHASE FAULT

A computer simulation of the network shown in Fig. 3 was performed using the 'Advanced Transient Program' (ATP Draw), a software package which is well recognised worldwide for performing power systems analysis. The purpose of a computer simulation was to gain a better understanding of how the induction generator in the fault path would replicate the NGT LVRT profile for a given fault condition. Fig. 5 shows the ATP layout.
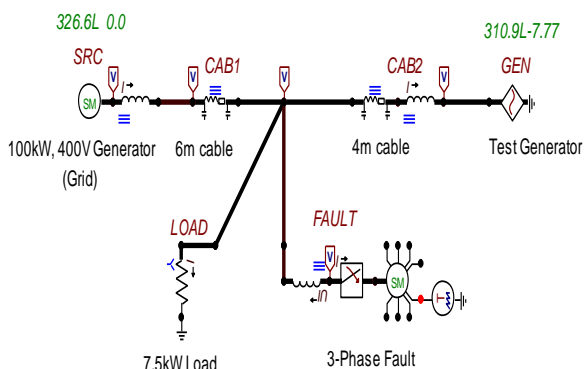
326.6L 0.0　　　　　　　　　　　　　　*310.9L-7.77*

Fig. 5

The ATP model uses the following data
Generator data (grid)
Rating = 100kVA
Voltage rating = 400V
Frequency = 50Hz
Power Factor = 0.8
X_d = 2.7 p.u.　　　X_q = 1.3 p.u.
$X'd$ = 0.26 p.u.　　$X''d$ = 0.145 p.u.
$X''q$ = 0.161 p.u.
X_2 = 0.153 p.u.　　X_0 = 0.03 p.u.
$T'do$ = 0.75sec　　$T'd$ = 0.07 sec
$T''d$ = 0.011 sec T_a = 0.012 sec
Inertia = 1.13kgm^2

Fault path induction machine data
Rating = 22kW
Voltage rating = 400V
Frequency = 50Hz
Speed = 1465 rpm
Power factor at full load = 0.83
Power factor at 1/2 load = 0.69
Current (In) = 42A
Efficiency = 90.8%
Torque ratio = 2.4
Current ratio = 6.3
Breakdown torque = 2.5
Inertia = 0.11kgm^2

$X''d$, $X'd$ and X_d are the respective machine reactances in the sub-transient, transient and steady states. X_2 and X_0 are the negative and zero sequence reactances, respectively. $T'do$ is the transient open circuit time constant. $T''d$ and $T'd$ are the respective sub-transient and transient short circuit time constants. T_a is the d.c. asymmetrical fault current time constant.

Cable data (grid generator & test generator)
Length : 6m (grid gen), 4m (test gen)
Resistance : 0.494mΩ/m
Reactance : 0.331µH/m

Figs. 6a and 6b show a typical voltage and current output, respectively when a 3-phase fault is applied. These were measured at points 1 and 2 respectively as shown in Fig. 3.

A 3-phase fault is applied at time t=0.5 seconds and is cleared at time t=1.6 seconds. Variation in voltage drop (ramp) can be represented by applying a variable inductance prior to fault clearance. This can be achieved by passing the fault current through an induction machine stator winding, then accelerating the machine from standstill to rated speed (in the example, between 1 – 1.5 seconds). The machine inductance increases as it reaches rated speed.
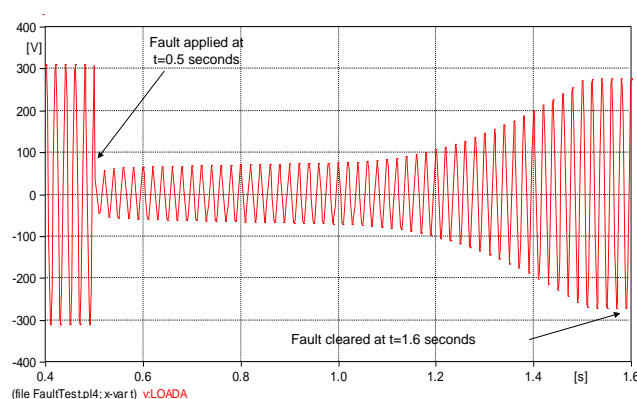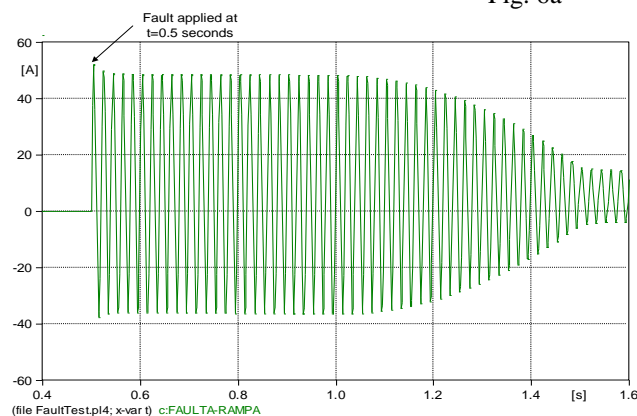

Fig. 6a

Fig. 6b

LABORATORY TEST SET-UP FOR A 3-PHASE FAULT

Fig. 7 shows the laboratory layout of the test rig. A 100kVA, 400V machine represents a grid supply feeding a resistive load bank. The DG machine under test is connected in parallel with the grid supply. The fault level / voltage dip is controlled via a combination of two sets of 3 single-phase inductors and an induction machine. The source inductance limits the fault level magnitude at the main bus feeding the load. The second inductance in the fault path acts like a voltage divider to set the ratio that dictates depth of voltage drop during the fault period. Also in the fault path is the stator winding of an induction

machine which is used to vary the fault impedance, mimicking the envelope of the fault ride through profile. This induction machine is run up to rated speed during the fault period. (This could be replaced by a suitably rated programmable impedance if available). The fault and voltage dip 'ramp' is triggered via timers. By altering the induction machine acceleration varies the voltage drop duration. This setup allows the test engineer to vary the fault duration, depth of voltage drop and the required rate of recovery, in one single test run.
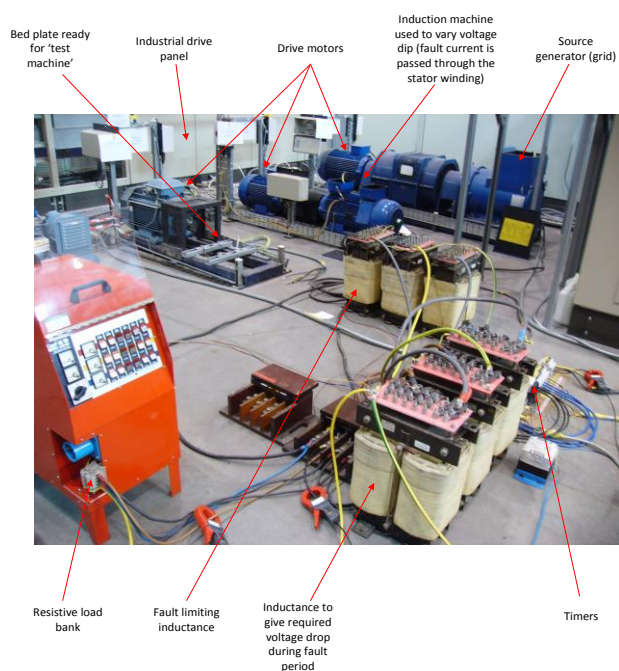

Fig. 7

Fig. 8 shows the timing diagrams for the fault control circuit
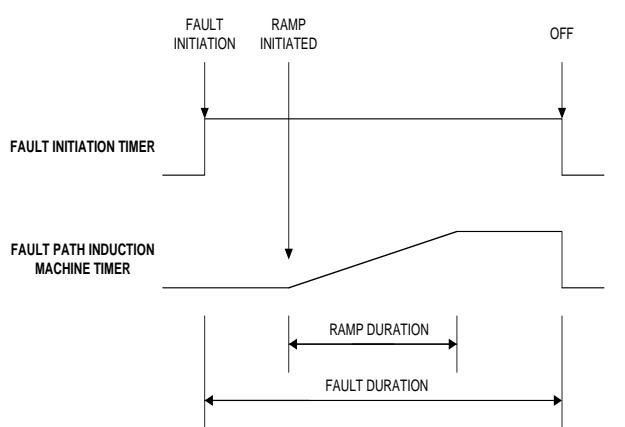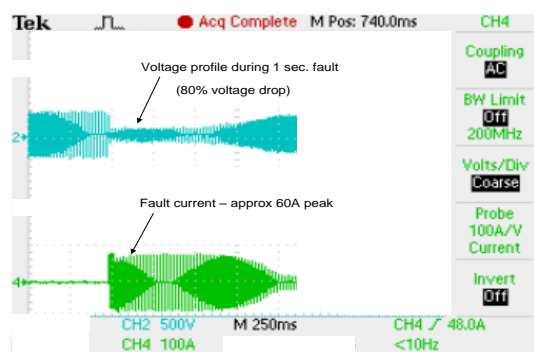

Fig.8

Fig. 9

Note that there will always be some fault impedance whilst having the induction motor (stator windings) connected in the fault path. However for solid faults, all series inductance including the induction machine was removed from the circuit.

SUMMARY
To support various grid code requirements currently being adopted throughout the world, Narec has been successful in simulating and practically implementing a laboratory setup that connects proto-type embedded generation onto a simple electrical network to test variable fault / voltage dip conditions. The method adopted provides a simple way to test performance at any or every point along the LVRT profile boundary giving the opportunity to initiate and clear a fault at any time and also to vary the voltage recovery. By repeating tests at various initial conditions, the region within the LVRT requirement envelope can be tested with one set of kit without constantly having to vary impedances between test runs, and in this way creates a very efficient test procedure.

FUTURE WORK
The setup described in this paper represents a relatively simple method to replicate low level fault conditions for scaled down proto-type machines only. The fault is triggered using a switch and has no point-on wave control. A future modification to the test rig would be to adopt point-on-wave control to ensure that the fault is initiated representing the most onerous condition, i.e. initiated at a voltage zero.

REFERENCES
[1] UK National Grid Code, Issue 2, Revision 4, Oct 2010
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[3] M.G. Say, 1958, Performance and Design of Alternating Current Machines. Pitman Publishing, London, UK