

PARAMETER COORDINATION OF MODULAR MULTILEVEL CONVERTER FOR ROBUST DESIGN DURING DC POLE TO POLE FAULT

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ABSTRACT

Sub-module over-current caused by dc pole-to-pole fault in modular multilevel converter based HVDC (MMC based HVDC) system is one of the important research objects about its electrical characteristics. In this paper, the fault mechanism before and after the converter blocked was analyzed respectively and the circuit model for the analysis of sub-module over-current was explored. The analytic equation for over-current calculation was deduced and a detailed analysis was also performed. The results indicate that the sub-module over-current is the ac system three phase short circuit current superposed the discharging current before the converter blocked, and the sub-module over-current is the ac system three phase short circuit current superposed the valve reactor freewheeling current after the converter blocked. The appropriate valve reactance and sub-module capacitance slow down the rate of fault current rise to leave enough time for the protection. This paper provides references for sub-module components electrical design.

INTRODUCTION

For many years of successful application in traction and medium voltage drive systems, the VSC (Voltage-Sourced Converter) utilizing modern IGBTs (Insulated Gate Bipolar Transistors) has become important in power transmission and distribution such as HVDC (High voltage Direct Current) and FACTS (Flexible Alternate current Transmission Systems) applications.

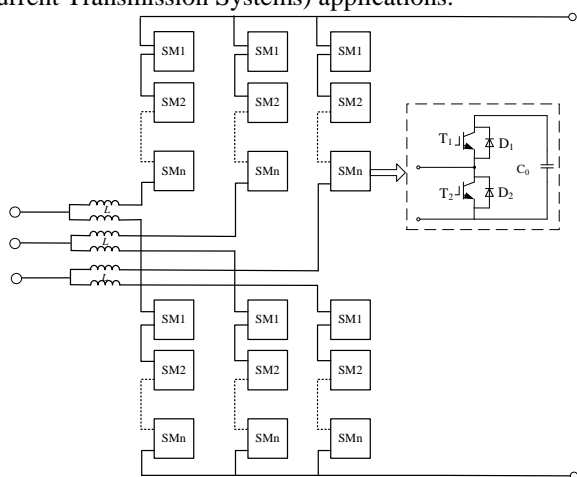


Fig. 1 Topology of MMC

A new MMC (modular multilevel converter) topology has been introduced into VSC based HVDC applications in recent years^[1]. Its arms act as controllable voltage sources with a high number of possible discrete voltage steps. A very smooth and nearly ideal sinus waveform can thus be generated with MMC converters. Each of these variable voltage sources is designed with a number of identical but individually controllable sub-modules, shown in Fig. 1^[2].

The engineering design of the MMC should not only stabilize the normal operation, but also ensures the converter operates within enough safety margins during the ac and dc side faults. Sub-module over-current caused by dc pole-to-pole fault in MMC based HVDC system is one of the important stresses that should be considered during design. Reasonable parameter coordination offers the protection enough time to cut off the over-current flowing through the switch devices.

This paper gives an insight into the dc pole to pole fault mechanism before and after the converter blocked. Then the circuit models for calculation of the sub-module over-current are explored. Based on the circuit models the over-current and the current rise time can be calculated. According to the above models and equations the engineers can understand the principle of the arm parameters coordination easily and choose the appropriate value for the project robust design.

FAULT MECHANISM

The bipolar cable dc lines are almost used in all the existing VSC-HVDC projects. This paper focuses on the dc cable pole to pole fault, which is permanent and has nothing to do with grounding arrangement.

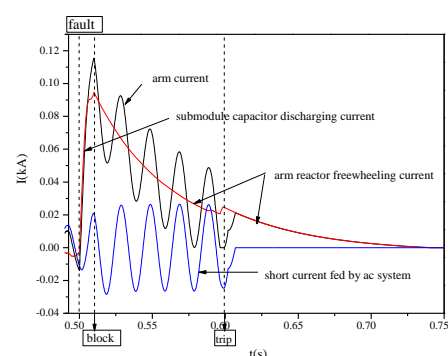


Fig. 2 Decomposition graph of the arm current

The dc pole-to-pole fault causes the sub-module dc capacitor to discharge; meanwhile the sub-module suffers the over-current fed by ac system, shown in Fig. 2. However, the current rate of rise is suppressed by the valve reactor, which gives enough time for the protection to block the converter. After blocking, only the diode D_2 suffers the short-circuit current.

Circuit model before blocking

The number of sub-modules with full module voltage in one phase unit is always ‘ n ’ before the converter blocking, so the equivalent capacitance of a phase is C_0/n . Thus the nonlinear switching process of the sub-modules can be neglected and the superposition principle can be applied.

The sub-module dc capacitor in one phase discharging equivalent circuit is shown in Fig. 3. The discharging current flowing through the IGBT T_1 , the valve reactor and the stray resistor, see Fig. 3(a). This is a typical second order circuit, so can be solved according to the circuit in Fig. 3(b). The two valve reactors in series of a phase is represented by $2L$. And $2C_0/n$ equal to the discharging capacitance because all the dc capacitor of upper and lower arm would discharge if the converter was not blocked. The stray resistor of a phase is R_{stray} .

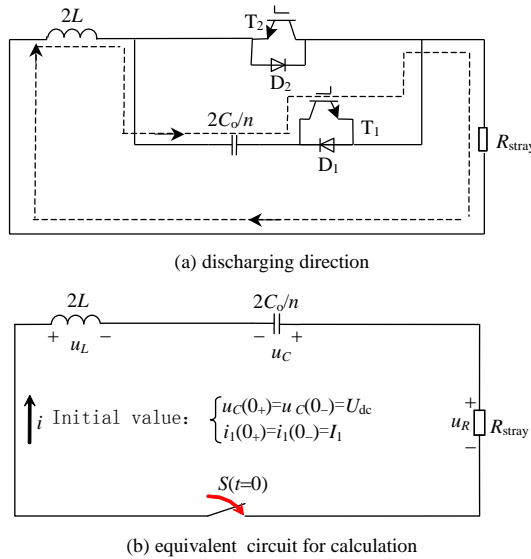


Fig. 3 Single phase equivalent circuit of Sub-module capacitors discharging

Due to the real R_{stray} is much less than $2\sqrt{nL/C_0}$, the discharging process is oscillating. The initial conditions are shown in Fig. 3(b). So the total capacitor voltage is

$$u_c = e^{-\frac{t}{\tau_1}} \left[\frac{U_{dc}\omega_0}{\omega} \sin(\omega t + \alpha) - \frac{nI_1}{2\omega C_0} \sin(\omega t) \right] \quad (1)$$

where τ_1 is the time constant for the discharging current attenuation, ω_0 is the natural frequency, ω is the

oscillating current angular frequency, and α is the oscillating current initial phase angle. All the above is determined by the circuit parameters:

$$\tau_1 = \frac{4L}{R_{stray}} \quad (2)$$

$$\omega_0 = \frac{1}{2} \sqrt{\frac{n}{LC_0}} \quad (3)$$

$$\omega = \frac{1}{2} \sqrt{\frac{n}{LC_0} - \left(\frac{R_{stray}}{2L}\right)^2} \quad (4)$$

$$\alpha = \arctan\left(\sqrt{\frac{4nL}{C_0 R_{stray}^2} - 1}\right) \quad (5)$$

Generally, $(R_{stray}/2L)^2$ is far below n/LC_0 , then ω is almost equal to ω_0 .

According to the relationship between the current and voltage of a capacitor, the discharging current can be deduced as

$$i_1 = e^{-\frac{t}{\tau_1}} [U_{dc} \sqrt{\frac{C_0}{nL}} \sin(\omega t) + I_1 \cos(\omega t)] \quad (6)$$

Define $\beta = \arctan\left(\frac{I_1}{U_{dc}} \sqrt{\frac{nL}{C_0}}\right)$, so equation (6) is changed to

$$i_1 = e^{-\frac{t}{\tau_1}} \left[\sqrt{\frac{C_0}{nL}} U_{dc}^2 + I_1^2 \sin(\omega t + \beta) \right] \quad (7)$$

The discharging current peak value increases with the increase of its initial absolute value.

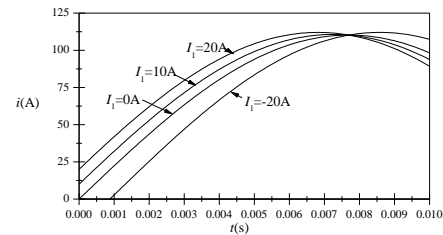


Fig. 4 Relationship between the discharging current and its initial value

If the ac bus of converter substation is far away from the power plant, the generator fault transient could be neglected. But the reverse is not true. So taking the fault current fed by the ac system into account, the real peak current is

$$I_{peak} = \sqrt{\frac{C_0}{nL} U_{dc}^2 + I_1^2} + \frac{\hat{I}_{3-fault}}{2} \quad (8)$$

Circuit model after blocking

The single phase equivalent circuit after blocking is illustrated in Fig. 5, where u_s is the equivalent source

phase voltage, L_{eq} represents the equivalent reactance and R_{eq} equals to the equivalent resistant between the source and the converter. D_{up} means all of D_2 in the upper arm, and D_{down} refers to the lower arm.

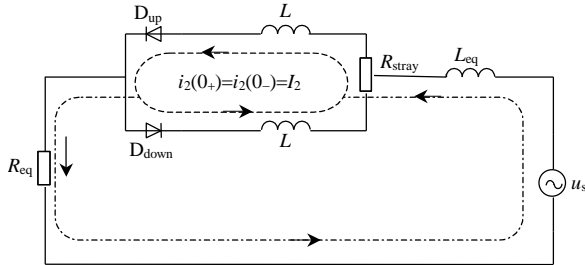


Fig. 5 Single phase equivalent circuit of the substation after blocking the converter

The changed circuit configuration caused two transient processes. 1) The capacitor discharging converts to the reactor freewheeling (see the dashed line in Fig. 5); 2) The current from the ac system just passes through D_2 (see the dash dotted line in Fig. 5).

The diodes D_2 conduct until the freewheeling current decrease to 0, so the equivalent is one order. Assume $u_s = \sqrt{2}U_s \sin(\omega_n t)$, in which ω_n is angular line frequency. Then the upper arm current is expressed as

$$i_{2up} = -\frac{\sqrt{2}U_s}{2|Z|} \cos(\omega_n t + \gamma) + I_2 e^{-\frac{t}{\tau_2}} \quad (9)$$

where

$$\tau_2 = \frac{2L}{R_{stray}} \quad (10)$$

$$|Z| = \sqrt{(R_{eq} + R_{stray}/4)^2 + \omega_n^2 (L_{eq} + L/2)^2} \quad (11)$$

$$\gamma = -\arctan \frac{\omega_n (L_{eq} + L/2)}{R_{eq} + R_{stray}/4} \quad (12)$$

The lower arm current is deduced to

$$i_{2down} = \frac{\sqrt{2}U_s}{2|Z|} \cos(\omega_n t + \gamma) + I_2 e^{-\frac{t}{\tau_2}} \quad (13)$$

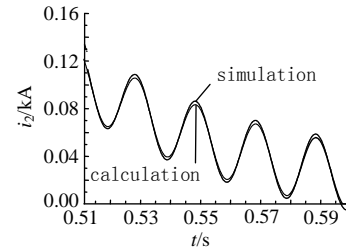
Due to the unilateral diode, the arm current will reverse after the freewheeling current changes to 0. In the fault steady-state the dc offset appears. When $R_{eq} = R_{stray} = 0$, the largest current is

$$i_{3up} = \frac{\sqrt{2}U_s}{2(\omega_n L_{eq} + \omega_n L/2)} [1 - \cos(\omega_n t)] \quad (14)$$

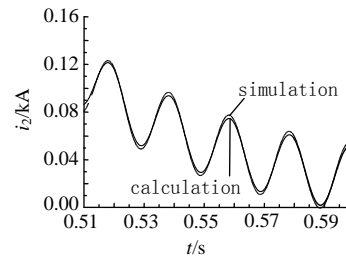
$$i_{3down} = \frac{\sqrt{2}U_s}{2(\omega_n L_{eq} + \omega_n L/2)} [1 + \cos(\omega_n t)] \quad (15)$$

However the breaker has tripped before the fault steady-state and the current becomes lower. So it is not the emphasis in real project.

Fig. 6 gives the arm current simulation and calculation curve after blocking the converter but before the fault steady-state. The calculation conforms to the simulation. It could be concluded that the method is feasible.



(a) upper arm current



(b) lower arm current

Fig. 6 Upper and lower arm current after blocking the converter

PARAMETER ROBUST DESIGN

In fact the converter is blocked within several *ms*. What suffers the most serious over-current stress is the diode D_2 in sub-modules. The diodes are protected by the parallel thyristor. The appropriate parameters should be chosen for the sub-module dc capacitors and valve reactors in order to leave enough time for the protection to act.

The equation (7) can be used in engineering design. Fig. 7 shows the discharging current with different sub-module capacitance. The discharging current is almost the same before 3 *ms*. So the valve reactance is decisive.

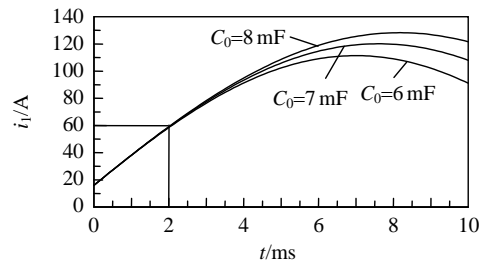


Fig. 7 Discharging current with different sub-module capacitance

If the maximum valve reactance still cannot meet the protection requirement, the sub-module dc capacitance should be reduced. The largest arm current rise time is

$$t_{\text{rise,max}} = 2\sqrt{\frac{LC_{0\text{max}}}{n}} \arctan\left[\frac{U_{\text{dc}}}{I_0} \sqrt{\frac{C_{0\text{max}}}{nL}}\right] \quad (16)$$

CONCLUSIONS

This paper researched on the dc pole to pole fault in MMC based HVDC. The results indicate that the sub-module over-current is the ac system three phase short circuit current superposed the discharging current before the converter blocking, and the sub-module over-current is the ac system three phase short circuit current superposed the valve reactor freewheeling current after the converter blocking.

The valve reactance is the main factor to decide the fault current rise time and can be calculated by an analytic equation.

The valve reactance should be coordinated by the sub-module dc capacitance to ensure a robust protection system.

APPENDIX A

1) Simulation parameters in PSCAD model

The ac terminal voltage: 105V;

Transformation ratio: 105V/332V;

Valve reactance: 14mH;

Sub-module dc capacitance: 6000 μ F;

The diode turn-on loss equivalent resistance: 0.01 Ω .

2) Fault time setting

The fault is located at the converter dc bus. It begins at 0.5s. The converter is blocked at 0.51s and the trip time is 0.6s.

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- [2] Z. Q. Liu, Q. Song, W. H. Liu, 2010, "VSC-HVDC system based on modular multilevel converters", Automation of Electric Power Systems, vol. 34(2), 53-58(in Chinese).